

# The QuickLogic EOS<sup>™</sup> S3 Voice and Sensor Processing

Ultra-Low Power Always-On, Always-Aware Applications

RTC Clocks LDO ADC		ARM Cortex-M4 with FPU		SRAM	
SPI Slave SPI Master UART		DMA and FIFOs		eFPGA	
Low Power Sound Detector		Flexible			I <sup>2</sup> C/SPI
l <sup>2</sup> S	PDM to PCM	Fusion Engine	Sensor Manager		I <sup>2</sup> C
	PDM				

## **Target Applications**

Hearable, Wearable, Smartphone, Tablet and IoT applications with voice trigger and sensor management

#### **Benefits**

- Comprehensive integrated solution for concurrent voice and motion, environmental and biometric sensor processing
- Hard-coded Low-Power Speech Detection (LPSD) for industry's lowest power always-on listening
- 2-mic beam-forming and noisesuppression for high-accuracy Key-Phrase Detection (KPD) in noisy environments
- Acoustic Echo Cancellation (AEC)
- eFPGA for flexible design
- Ultra-low power biometric and motion sensor processing with dedicated µDSP (Flexible Fusion Engine)
- On/Off-body detection placing device in lowest power mode when not in use
- Low-Voltage (0.85 VDD) option for 33% power reduction

- Sensor Manager Autonomously manages and controls all sensors
- Flexible Fusion Engine<sup>™</sup> (FFE) 10 MHz DSP-like processor supports always-on computational processing at one fourth the power
- eFPGA Enables custom logic functions and I/O expansions
- Voice Processing Hard-coded Low Power Sound Detector (LPSD) and PDM to PCM conversion minimizes audio processing power
- ARM Cortex-M4 with FPU Up to 80 MHz and 512 KB SRAM for general purpose processing and running O/S
- Serial I/O SPI Master/Slave, I<sup>2</sup>C, UART
- System DMA, Integrated RTC, Oscillators, ADC, LDO

### **Key Features**

- Cortex M4-F Processor (up to 80 MHz operating frequency)
- µDSP-like Flexible Fusion Engine (FFE)
  - 10 MHz operating frequency
  - Dedicated 50 KB SRAM Prog, 16 KB SRAM Data
- 512 KB SRAM
- Hardware Sensor Manager
  - Autonomous initialization and sampling of sensors
- Power Management Unit (PMU)
- SPI Master/Slave, I2S Master/Slave & I2C
- eFPGA
  - 2,400 effective logic cells with 64 Kbits of available RAM
  - Eight RAM FIFO controllers
- 12 bit ADC
- PDM Mic Support with dedicated logic for PCM conversion
- Dual Low-Dropout (LDO) regulators

## Packaging

- 42 WLSCSP (2.7 x 2.4 x 0.7 mm)
- 64-Ball BGA (3.5 x 3.5 x 0.8 mm)

For more information, please visit www.quicklogic.com