ArcticLink® III VX6 Solution Platform Data Sheet

Dual Output High Definition Visual Enhancement Engine (VEE HD+) and Display Power Optimizer (DPO HD+) Solution

Platform Highlights

High Definition Visual Enhancement Engine

- VEE HD+ compensates for different viewing environments by restoring and enhancing the display content through contrast and dynamic range optimization.
- Greatly enhanced image and video quality even under low backlight or bright ambient conditions.
- Supports up to WUXGA (1920x1200).
- Based on proven, patented technology, licensed from Apical Ltd.

High Definition Display Power Optimizer

- Dramatically improves battery life up to 50% by reducing liquid crystal display (LCD) backlight or organic light-emitting diode (OLED) brightness.
- Tightly coupled with the VEE HD+ technology for optimal operation.
- Directly controls the pulse-width modulation (PWM) for backlight management.
- Integrated Intelligent Brightness Control (IBC) feature allows up to an additional 10% power savings by modulating display brightness based on display content.

Serial Peripheral Interface (SPI) Master

- Serial interface to control sensors, peripherals, and/or displays.

I²C Client

- CPU interface for configuring and controlling internal VEE HD+ registers, DPO HD+ registers and look-up tables (LUT).

NOTE: The MIPI interface can also be used instead of I²C.

Onboard Clock Generation

- Integrated, very low power phase-locked loop (PLL) for generating the clocks necessary for VEE HD+.

Small Form Factor Packaging

- 120-ball, 4.5 mm x 4.5 mm WLCSP, 0.4 mm ball pitch.

Display Interface Bridging

- The ArcticLink III VX6 solution platform performs on-chip bridging of the MIPI processor to display MIPI, LVDS interfaces.

Applications Overview

The ArcticLink III VX6 solution platform consists of the following main modules:

- VEE HD+
- DPO HD+
- Display interface bridging

This highly integrated, yet flexible architecture makes it the ideal platform to implement display path solutions for smartphones, tablets, and smartbooks.

The ArcticLink III VX6 solution platform can be used to replace several discrete components typically used in mobile devices today to reduce power consumption, reduce bill of materials (BOM) cost, and save precious printed circuit board (PCB) space.

High Definition Visual Enhancement Engine

The ArcticLink III VX6 solution platform embeds the VEE HD+ technology with very low power and optimal die size for lowest BOM costs. QuickLogic and Apical Limited partnered to architect and develop the optimal blend of algorithms and interfaces for mobile and portable multimedia products. The VEE HD+ technology is based on a proven core licensed from Apical Limited, which is substantiated by nearly a decade of scientific research. These algorithms implement a model of human perception; resulting in a displayed image that retains detail, color and vitality even under variable viewing conditions. It specifically addresses the problem of the low contrast ratio of mobile displays to bring a more TV-like viewing experience to the mobile devices.

The QuickLogic proprietary VEE HD+ solution substantially enhances image and video quality by optimizing the dynamic range, contrast, and color saturation pixel-by-pixel to provide a natural viewing experience under low backlight or bright ambient light conditions. Seamlessly integrated into the display path, the VEE HD+ technology enhances the user's mobile multimedia visual experience while DPO HD+ drastically reduces backlight power to extend battery life.

High Definition Display Power Optimizer

As consumer devices have become more power hungry, system designers are constantly looking for ways to lower system power consumption. As displays typically consume 30% to 60% of the total system power, there has been a tremendous amount of research put into methods of reducing display power. A common solution is to lower the backlight level of the LCD or average brightness level of an OLED. Unfortunately, this solution significantly diminishes the viewing experience since most details are lost due to the lowered contrast ratio.

While the VEE HD+ technology uses statistical information gathered pixel-by-pixel, frame-by-frame to adjust the value of individual pixels, DPO HD+ uses that same information to adjust the backlight or display brightness. The ability to provide a unique tone curve for each pixel and tight control over the display backlight gives greater flexibility than the global adjustments of alternative implementations. The QuickLogic approach results in greater power savings and the entirely new capability of adapting to a bright environment.

The ArcticLink III VX6 solution platform also contains the QuickLogic IBC feature, which allows additional battery savings by modulating the display brightness based upon actual display content. If the content being displayed is of a lower contrast or dynamic range (such as streamed video from popular internet video sites), display brightness can be lowered without affecting the viewing experience. This results in a system-level battery savings.

DPO HD+ seamlessly integrates with the QuickLogic VEE HD+, ensuring longer battery life and an excellent visual experience by coupling the PWM driving the display backlight with the display content processing parameters of the VEE HD+ technology.

Display Interface Bridging

The ArcticLink III VX6 features a MIPI input and dual MIPI/RGB, LVDS/RGB, or MIPI/LVDS outputs, enabling bridging of display interfaces on the device.

ArcticLink III VX6 Solution Platform Variants

The ArcticLink III VX6 solution platform features six distinct variants as described in **Table 1**.

Table 1: ArcticLink III VX6 Solution Platform Variants

QuickLogic Part Order Number	Part Number	Device Input	Device Output	Max. Resolution[a] (60 FPS)	Primary Application
CSSP-AUFDN120	VX6B2E	MIPI-2[b]	MIPI-2[b] and RGB	1366 x 768	Smartphones and tablets with pico projectors
CSSP-AEFDN120	VX6B3E	MIPI-4[c]	MIPI-4[c] and RGB	1920 x 1200	Smartphones and tablets with pico projectors
CSSP-BRFDN120	VX6B2G	MIPI-2[b]	LVDS-1[d] and RGB	1280 x 720	Tablets with pico projectors or secondary HDMI/MHL encoders
CSSP-BSFDN120	VX6B3G	MIPI-4[c]	LVDS-2[e] and RGB	1920 x 1200	Tablets with pico projectors or secondary HDMI/MHL encoders
CSSP-BYFDN120	VX6B2H	MIPI-2[b]	MIPI-2[b] and LVDS-1[e]	1280 x 720	Tablets with secondary HDMI/MHL encoders
CSSP-BZFDN120	VX6B3H	MIPI-4[c]	MIPI-4[c]and LVDS-2[f]	1920 x 1200	Tablets with secondary HDMI/MHL encoders

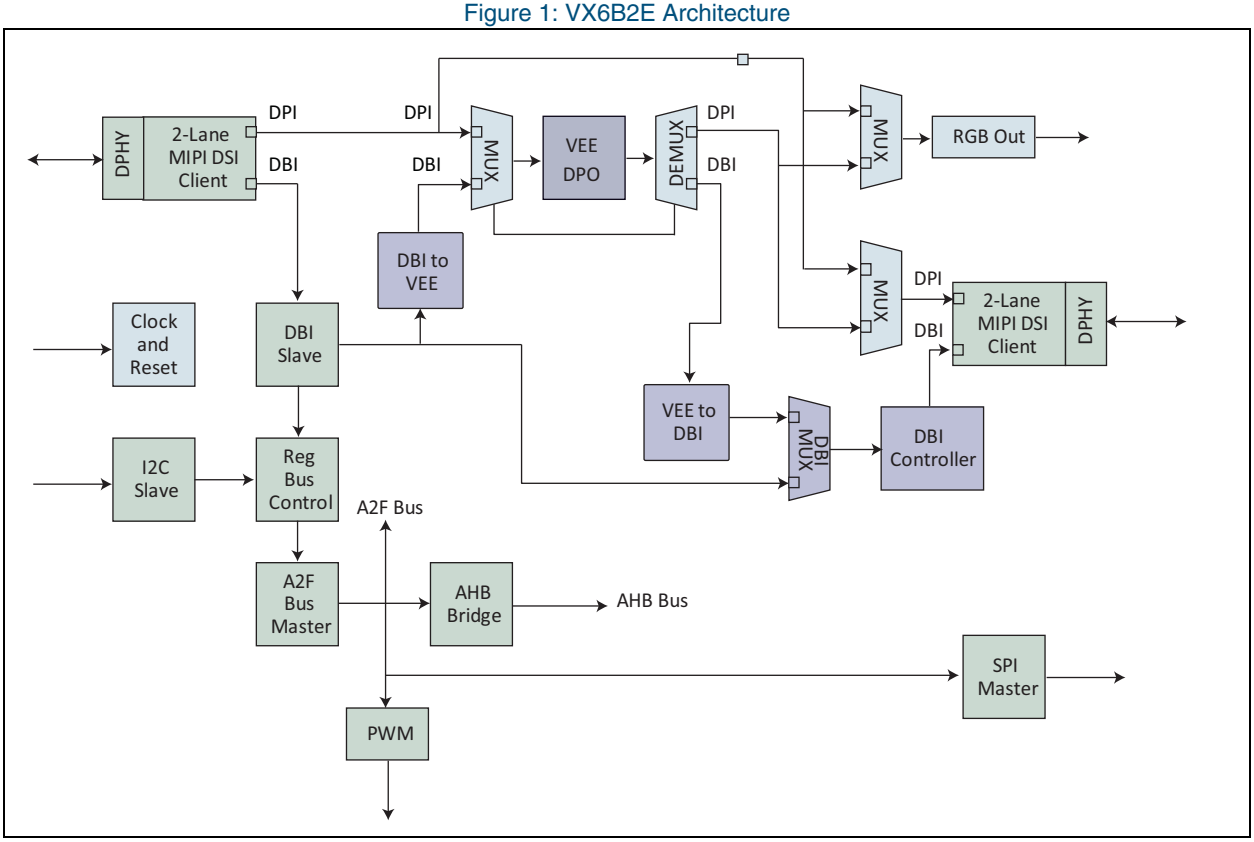
a. MIPI “video mode” only.
b. MIPI-2: Two lane MIPI.
c. MIPI-4: Four lane MIPI.
d. LVDS-1: One channel LVDS.
e. LVDS-2: Two channel LVDS

Data Paths

VX6B2E — MIPI-2 to MIPI-2 and RGB

CAUTION: Video data sent over MIPI command mode is limited to no more than FWVGA (854x480) resolutions.

Figure 1: VX6B2E Architecture



Use Case

Data path input and outputs are:

- Input – MIPI 2-lane
- Output – MIPI 2-lane and RGB

Control path input and outputs are:

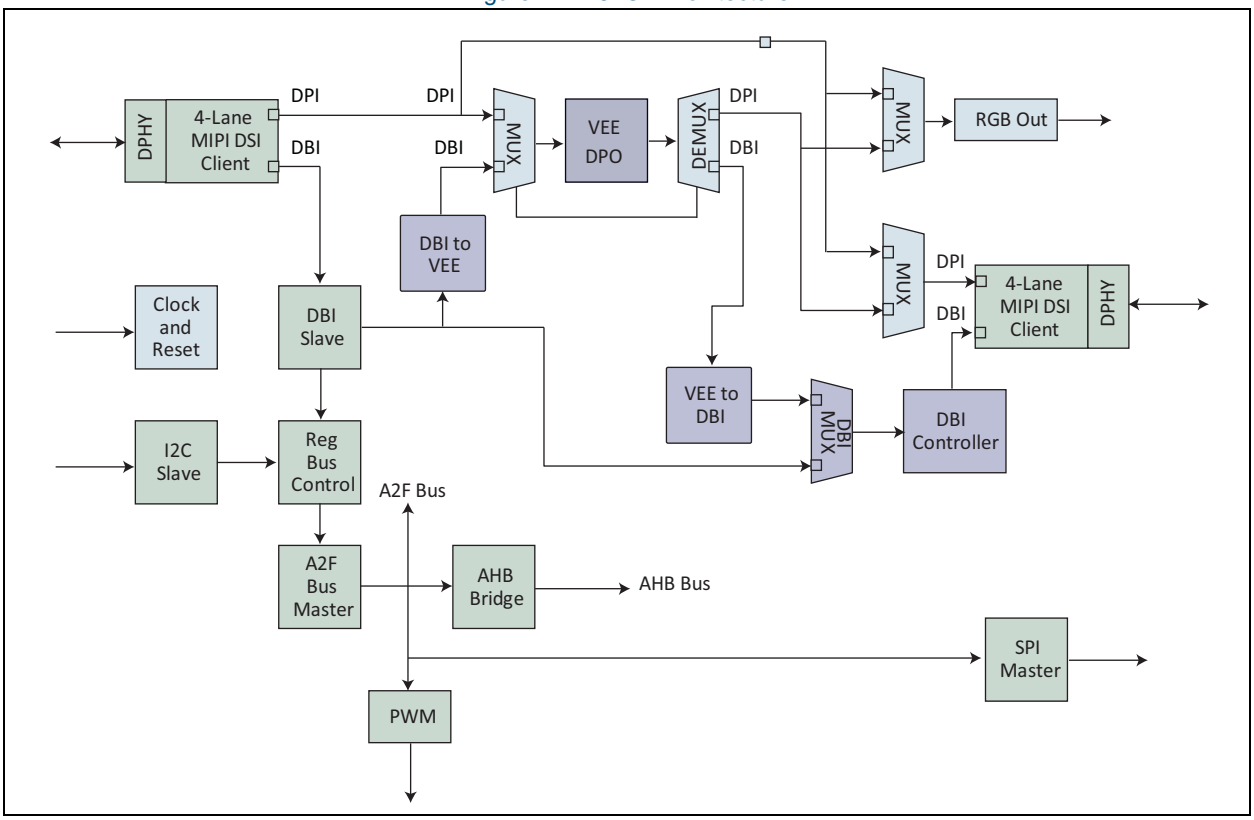
- Input – I^2C and/or MIPI DBI
- Output – SPI and/or MIPI DBI

Maximum resolution is WXGA (1366 x 768) at 24 bpp at 60 fps. The speed is limited by MIPI bandwidth.

VX6B3E — MIPI-4 to MIPI-4 and RGB

CAUTION: Video data sent over MIPI command mode is limited to no more than FWVGA (854x480) resolutions.

Figure 2: VX6B3E Architecture



Use Case

Data path input and outputs are:

- Input – MIPI 4-lane
- Output – MIPI 4-lane and RGB

Control path input and outputs are:

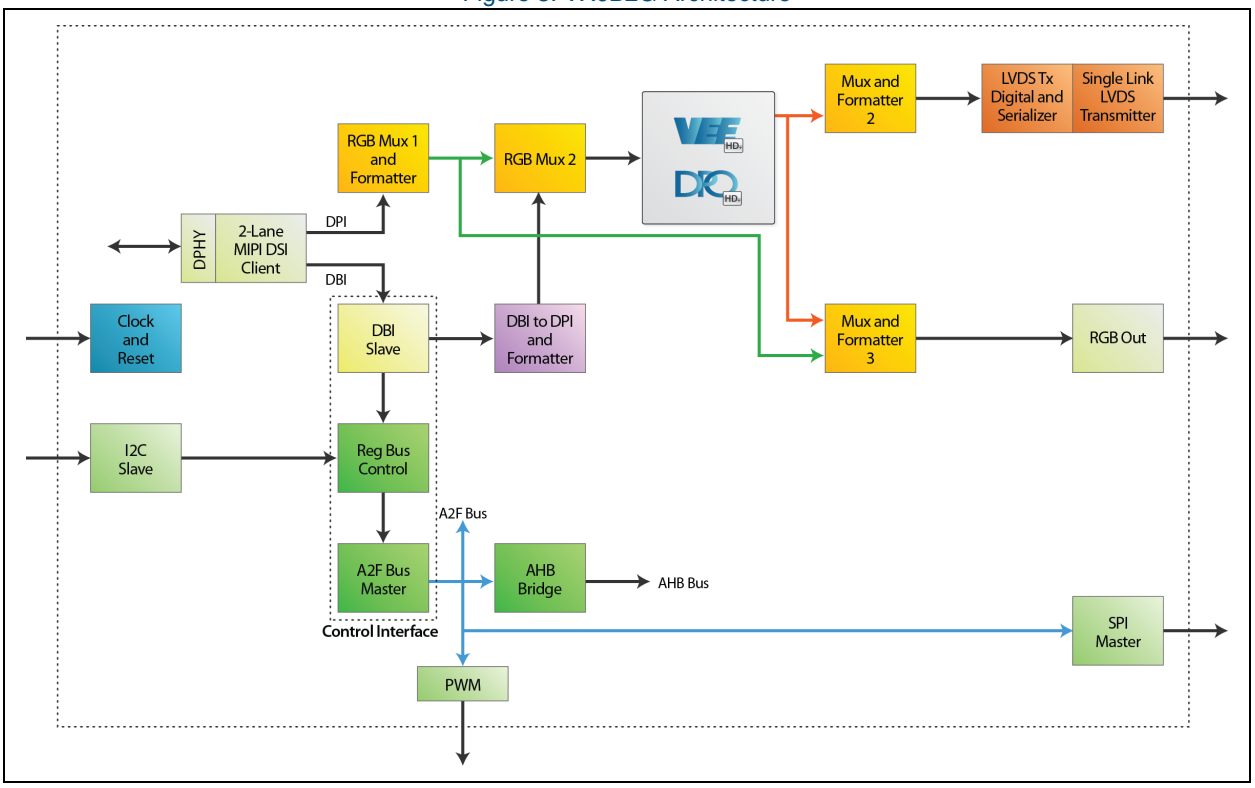
- Input – I^2C and/or MIPI display bus interface (DBI)
- Output – SPI and/or MIPI DBI

Maximum resolution is WUXGA (1920 x 1200) at 24 bpp at 60 fps. The speed is limited by MIPI bandwidth.

VX6B2G — MIPI-2 to LVDS-1 and RGB

CAUTION: Video data sent over MIPI command mode is limited to no more than FWVGA (854x480) resolutions.

Figure 3: VX6B2G Architecture



Use Case

Data path input and outputs are:

- Input – MIPI 2-lane
- Output – RGB and LVDS-1

Control path input and outputs are:

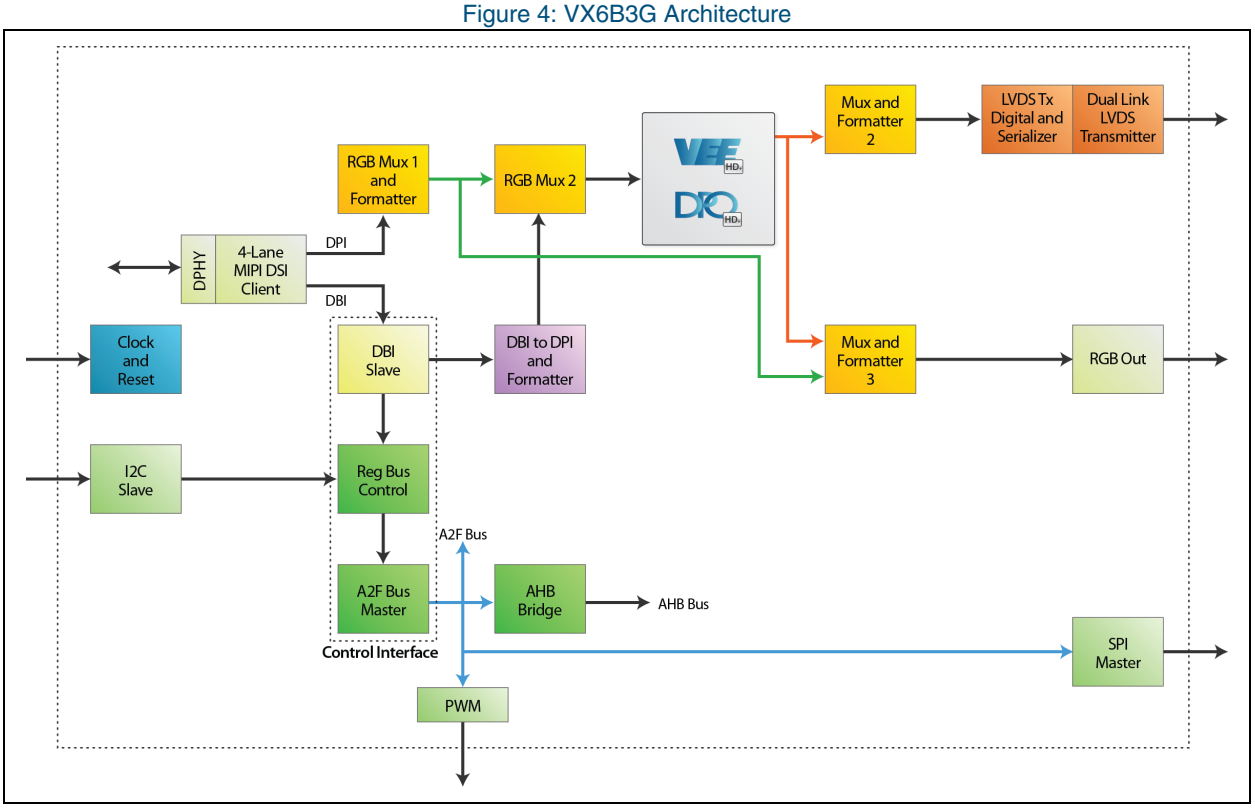
- Input – I^2C and/or MIPI DBI
- Output – SPI

Maximum resolution is 1280 x 720 at 24 bpp at 60 fps. The speed is limited by LVDS bandwidth.

VX6B3G — MIPI-4 to LVDS-2 and RGB

CAUTION: Video data sent over MIPI command mode is limited to no more than FWVGA (854x480) resolutions.

Figure 4: VX6B3G Architecture



Use Case

Data path input and outputs are:

- Input – MIPI 4-lane
- Output – RGB and LVDS-2

Control path input and outputs are:

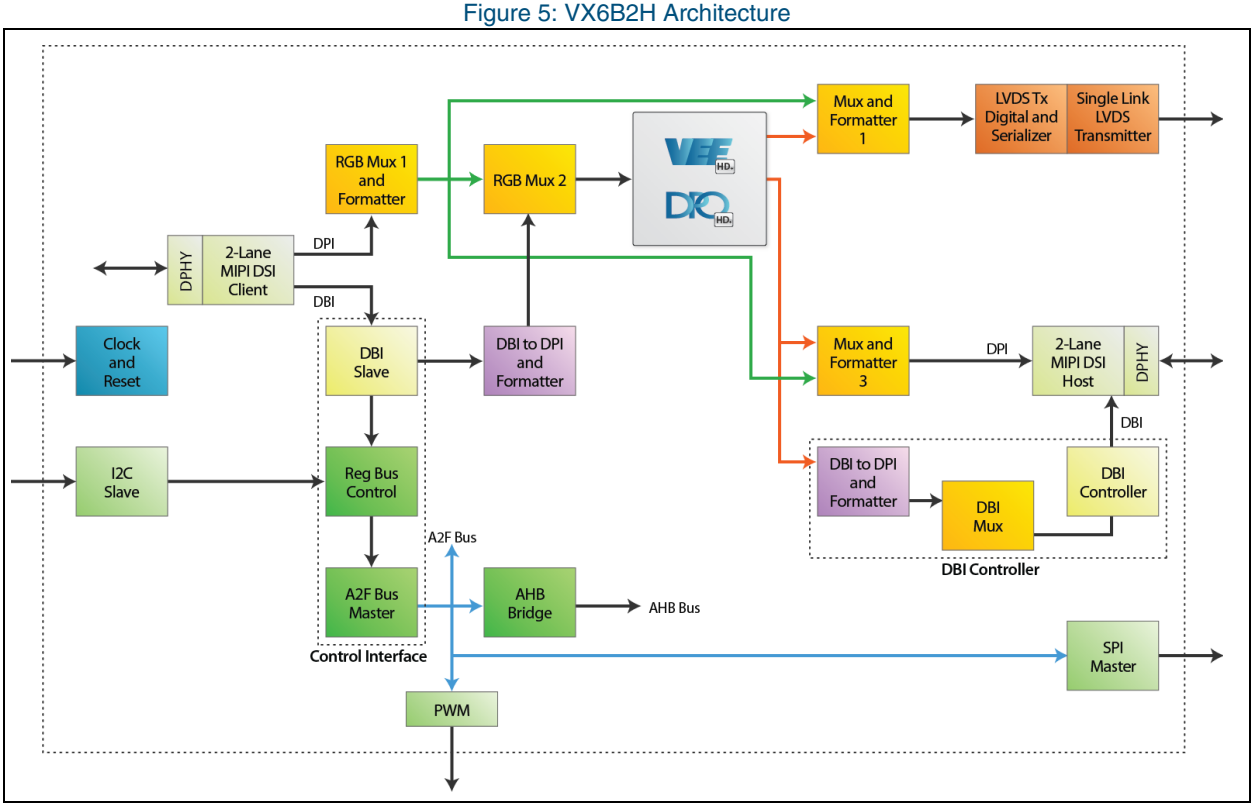
- Input – I^2C and/or MIPI DBI
- Output – SPI

Maximum resolution is 1920 x 1200 at 24 bpp at 60 fps. The speed is limited by MIPI bandwidth.

VX6B2H — MIPI-2 to MIPI-2 and LVDS-1

CAUTION: Video data sent over MIPI command mode is limited to no more than FWVGA (854x480) resolutions.

Figure 5: VX6B2H Architecture



Use Case

Data path input and outputs are:

- Input – MIPI 2-lane
- Output – MIPI 2-lane and LVDS-1

Control path input and outputs are:

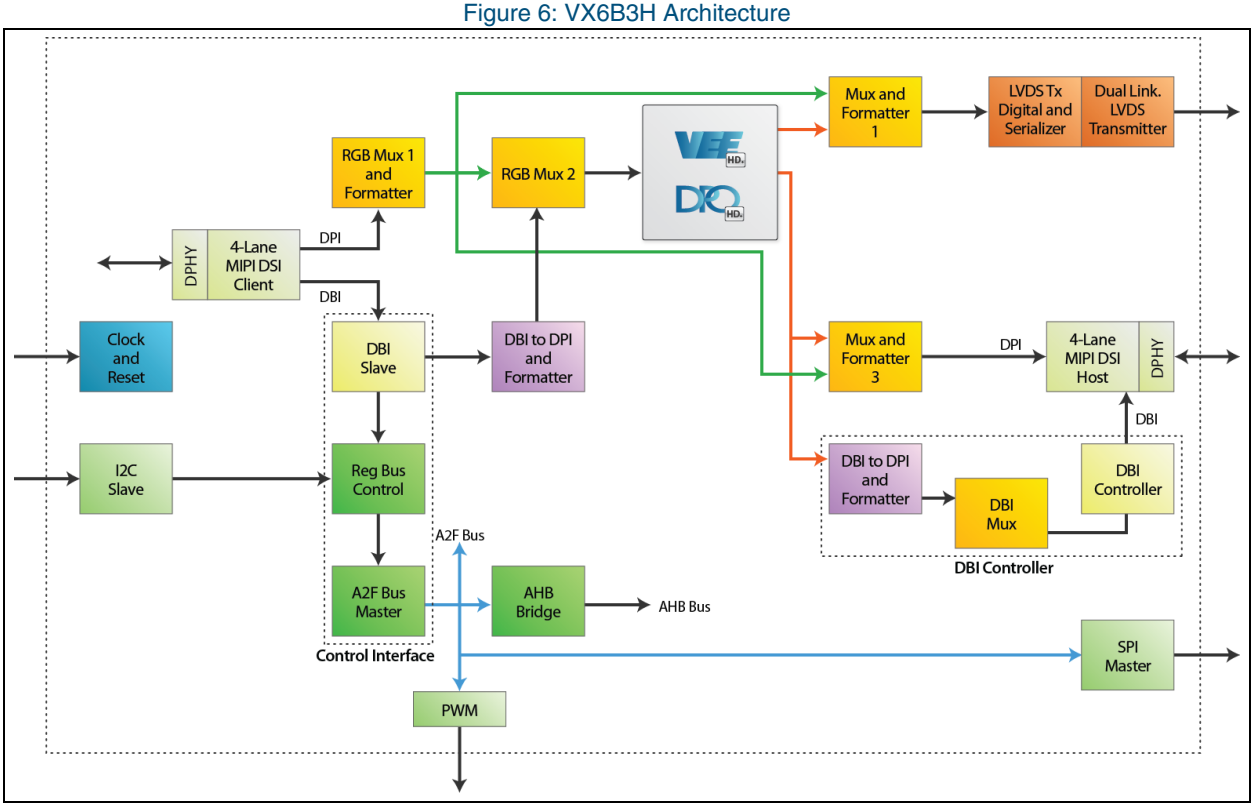
- Input – I^2C and/or MIPI DBI
- Output – SPI

Maximum resolution is 1280 x 720 at 24 bpp at 60 fps. The speed is limited by LVDS bandwidth.

VX6B3H — MIPI-4 to MIPI-4 and LVDS-2

CAUTION: Video data sent over MIPI command mode is limited to no more than FWVGA (854x480) resolutions.

Figure 6: VX6B3H Architecture



Use Case

Data path input and outputs are:

- Input – MIPI 4-lane
- Output – MIPI 4-lane and LVDS-2

Control path input and outputs are:

- Input – I^2C and/or MIPI DBI
- Output – SPI

Maximum resolution is 1920 x 1200 at 24 bpp at 60 fps. The speed is limited by MIPI bandwidth.

Power Consumption

Table 2 and **Table 3** shows the power consumption in various operating modes.

Table 2: VX6Bxx Power Consumption (mW) at 60 fps[a]

Resolution	Display Width (pixels)	Display Height (pixels)	VX6B2E		VX6B3E		VX6B2G		VX6B3G	
			18 bpp	24 bpp	18 bpp	24 bpp	18 bpp	24 bpp	18 bpp	24 bpp
QVGA	320	240	46.7	50.5	47.5	51.1	63.9	68.8	167.8	171.1
VGA	640	480	58.4	64.8	58.8	63.9	79.1	86.0	172.3	175.7
WVGA	854	480	64.4	71.8	63.5	69.1	85.4	93.0	175.2	178.7
PAL	768	576	67.2	75.0	65.6	71.5	88.3	96.2	175.9	179.4
SVGA	800	600	69.1	77.5	67.4	73.7	90.7	99.2	176.0	180.3
XGA	1,024	768	87.9	99.01	82.5	91.7	111.0	123.4	181.9	185.5
HD 720	1,280	720	94.5	107.3	88.3	98.4	118.8	132.4	184.1	187.7
WXGA	1,366	768	101.7	115.7	94.4	105.6	-	-	186.3	190.1
SXGA	1,280	960	113.9	-	105.0	117.7	-	-	190.8	194.6
SXGA	1,280	1,024	119.0	-	109.1	122.4	-	-	192.3	196.2
SXGA+	1,400	1,050	126.0	-	114.8	128.8	-	-	194.5	198.4
UXGA	1,600	1,200	-	-	138.4	156.5	-	-	203.6	228.4
HD 1080	1,920	1,080	-	-	145.0	163.7	-	-	224.6	231.2
WUXGA	1,920	1,200	-	-	156.6	177.1	-	-	229.3	236.1

a. MIPI DBI command mode is limited to FWVGA (854x480) maximum.

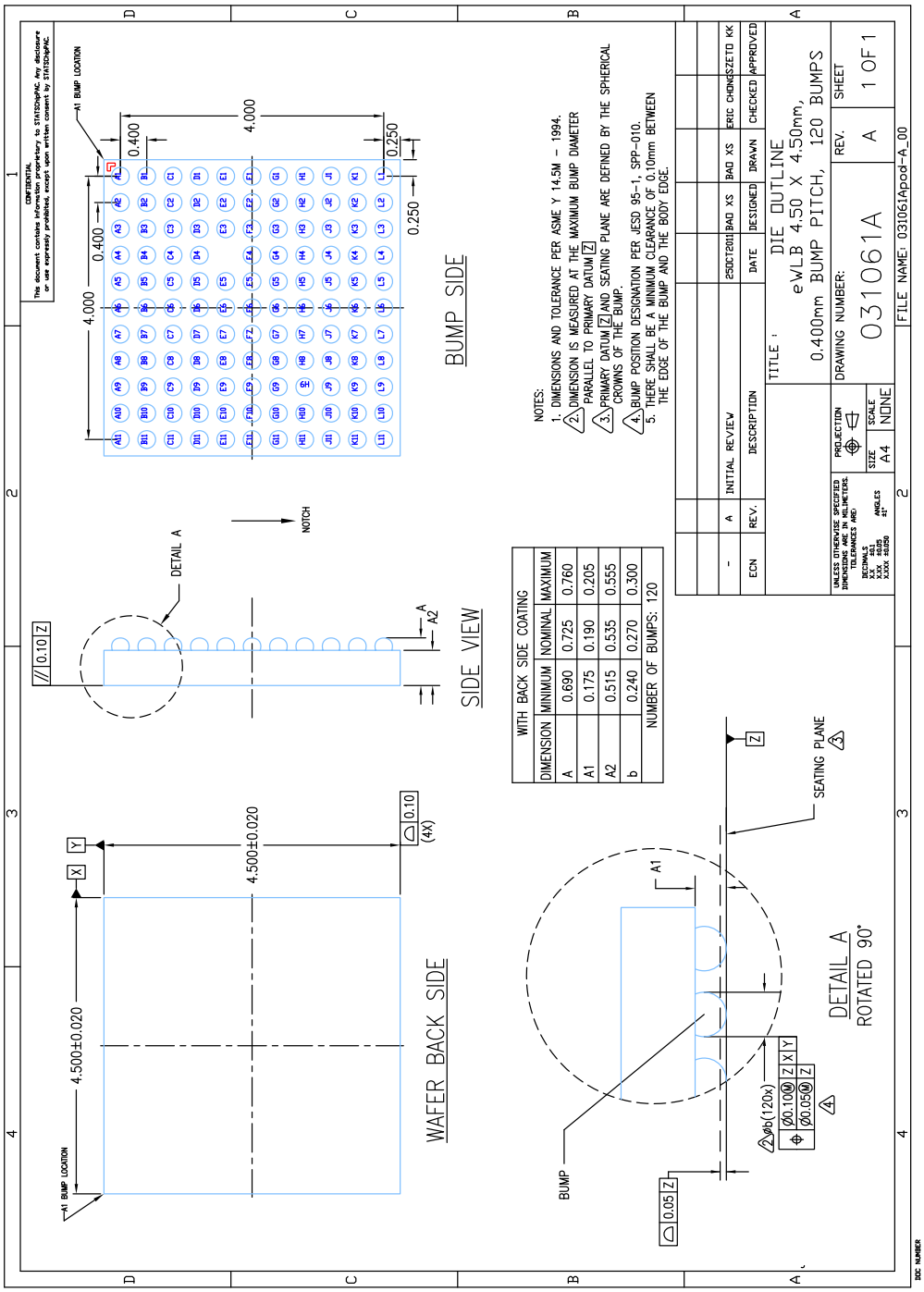
Table 3: VX6Bxx Power Consumption (mW) at 60 fps[a]

Resolution	Display Width (pixels)	Display Height (pixels)	VX6B2H		VX6B3H	
			18 bpp	24 bpp	18 bpp	24 bpp
QVGA	320	240	108.5	109	171.8	172.3
VGA	640	480	115.7	116.7	178.2	178.9
WVGA	854	480	119.4	120.7	180.7	181.9
PAL	768	576	120.7	122.5	182.8	182.8
SVGA	800	600	122.2	123.9	183.9	184.1
XGA	1,024	768	133.8	135.9	193.2	194.5
HD 720	1,280	720	137.8	140.5	196.9	198.2
WXGA	1,366	768	-	-	200.8	202.3
SXGA	1,280	960	-	-	207.6	209.6
SXGA	1,280	1,024	-	-	110.2	212.2
SXGA+	1,400	1,050	-	-	213.9	215.8
UXGA	1,600	1,200	-	-	228.8	231.8
HD 1080	1,920	1,080	-	-	233.0	235.9
WUXGA	1,920	1,200	-	-	240.4	243.5

a. MIPI DBI command mode is limited to FWVGA (854x480) maximum.

Mechanical Drawing

Figure 7: VX6 Solution Platform – CSSP 120 0.4 mm Ball (4.5 mm x 4.5 mm) WLCSP Mechanical Drawing



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Revision History

Revision	Date	Originator and Comments
1.0	October 2012	Initial production release.
1.1	February 2013	Paul Karazuba and Kathleen Bylsma Added two packages VX6B2G and VX6B3G
1.2	March 2013	Paul Karazuba and Kathleen Bylsma Added two packages VX6B2H and VX6B3HG
1.3	June 2013	Paul Karazuba and Kathleen Bylsma Updated contact information.
1.4	June 2016	Brian Faith and Kathleen Bylsma Added QuickLogic Part Order Number to Table 1.

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