ArcticLink® III VX5 Solution Platform Data Sheet

High Definition Visual Enhancement Engine (VEE HD+) and Display Power Optimizer (DPO HD+) Solution

Platform Highlights

High Definition Visual Enhancement Engine

- VEE HD+ compensates for different viewing environments by restoring and enhancing the display content through contrast and dynamic range optimization.
- Greatly enhanced image and video quality even under low backlight or bright ambient conditions.
- Supports up to WUXGA (1920x1200).
- Based on proven, patented technology, licensed from Apical Ltd.

High Definition Display Power Optimizer

- Dramatically improves battery life up to 50% by reducing liquid crystal display (LCD) backlight or organic light-emitting diode (OLED) brightness.
- Tightly coupled with the VEE HD+ technology for optimal operation.
- Directly controls the pulse-width modulation (PWM) for backlight management.
- Integrated Intelligent Brightness Control (IBC) feature allows up to an additional 10% power savings by modulating display brightness based on display content.

Serial Peripheral Interface (SPI) Master

- Serial interface to control sensors, peripherals, and/or displays.

Onboard Clock Generation

- Integrated, very low power phase-locked loop (PLL) for generating the clocks necessary for VEE HD+.

I²C Client

- CPU interface for configuring and controlling internal VEE HD+ registers, DPO HD+ registers and look-up tables (LUT).

Small Form Factor Packaging

- 120-ball, 4.5 mm x 4.5 mm WLCSP, 0.4 mm ball pitch.

Applications Overview

The ArcticLink III VX5 solution platform consists of the following main modules:

- VEE HD+
- DPO HD+

This highly integrated, yet flexible architecture makes it the ideal platform to implement display path solutions for smartphones, tablets, and smartbooks.

The ArcticLink III VX5 solution platform can be used to replace several discrete components typically used in mobile devices today to reduce power consumption, reduce bill of materials (BOM) cost, and save precious printed circuit board (PCB) space.

High Definition Visual Enhancement Engine

The ArcticLink III VX5 solution platform embeds the VEE HD+ technology with very low power and optimal die size for lowest BOM costs. QuickLogic and Apical Limited partnered to architect and develop the optimal blend of algorithms and interfaces for mobile and portable multimedia products. The VEE HD+ technology is based on a proven core licensed from Apical Limited, which is substantiated by nearly a decade of scientific research. These algorithms implement a model of human perception; resulting in a displayed image that retains detail, color and vitality even under variable viewing conditions. It specifically addresses the problem of the low contrast ratio of mobile displays to bring a more TV-like viewing experience to the mobile devices.

The QuickLogic proprietary VEE HD+ solution substantially enhances image and video quality by optimizing the dynamic range, contrast, and color saturation pixel-by-pixel to provide a natural viewing experience under low backlight or bright ambient light conditions. Seamlessly integrated into the display path, the VEE HD+ technology enhances the user's mobile multimedia visual experience while DPO HD+ drastically reduces backlight power to extend battery life.

High Definition Display Power Optimizer

As consumer devices have become more power hungry, system designers are constantly looking for ways to lower system power consumption. As displays typically consume 30% to 60% of the total system power, there has been a tremendous amount of research put into methods of reducing display power. A common solution is to lower the backlight level of the LCD or average brightness level of an OLED. Unfortunately, this solution significantly diminishes the viewing experience since most details are lost due to the lowered contrast ratio.

While the VEE HD+ technology uses statistical information gathered pixel-by-pixel, frame-by-frame to adjust the value of individual pixels, DPO HD+ uses that same information to adjust the backlight or display brightness. The ability to provide a unique tone curve for each pixel and tight control over the display backlight gives greater flexibility than the global adjustments of alternative implementations. The QuickLogic approach results in greater power savings and the entirely new capability of adapting to a bright environment.

The ArcticLink III VX5 solution platform also contains the QuickLogic IBC feature, which allows additional battery savings by modulating the display brightness based upon actual display content. If the content being displayed is of a lower contrast or dynamic range (such as streamed video from popular internet video sites), display brightness can be lowered without affecting the viewing experience. This results in a system-level battery savings.

DPO HD+ seamlessly integrates with the QuickLogic VEE HD+, ensuring longer battery life and an excellent visual experience by coupling the PWM driving the display backlight with the display content processing parameters of the VEE HD+ technology.

ArcticLink III VX5 Solution Platform Variants

The ArcticLink III VX5 solution platform features eight distinct variants as described in **Table 1**.

Table 1: ArcticLink III VX5 Solution Platform Variants

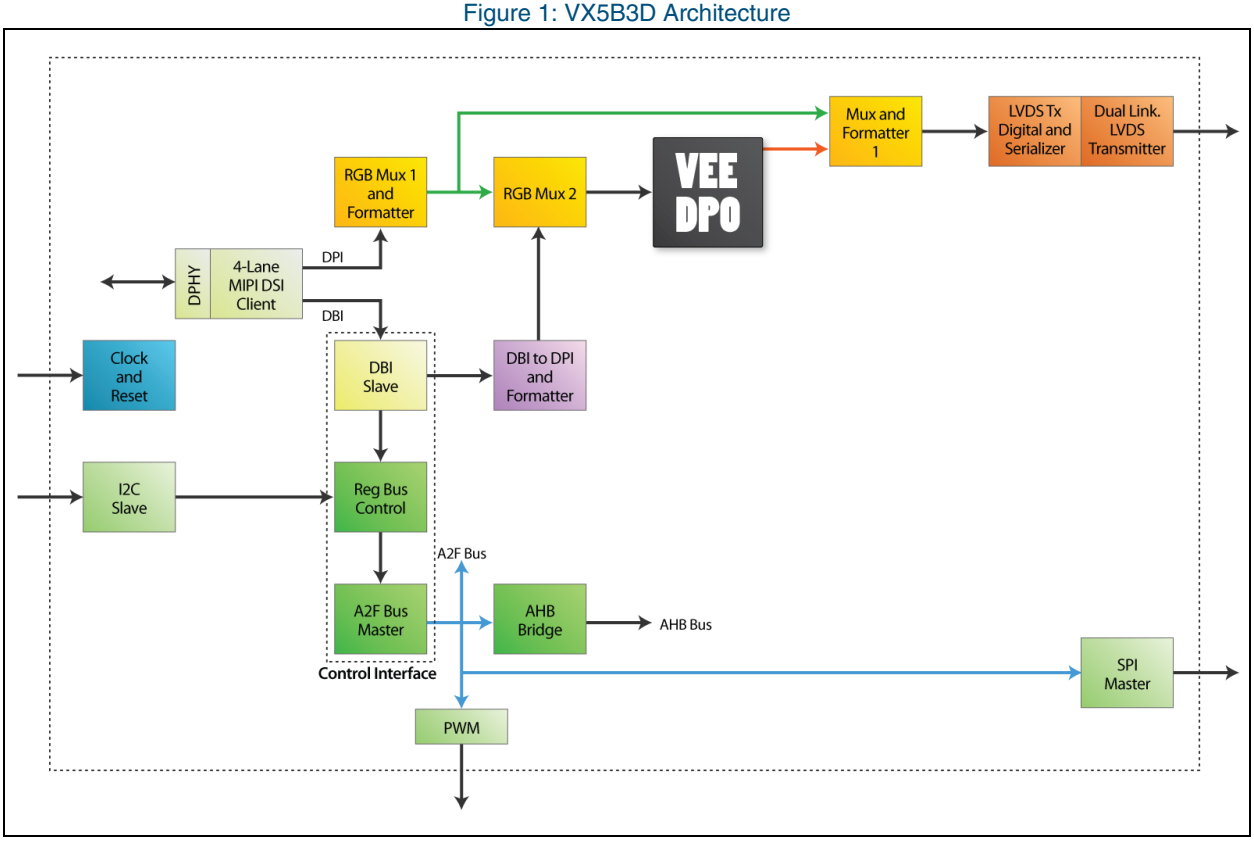
QuickLogic Part Order Number	Part Number	Device Input	Device Output	Max Resolution (60 FPS)	Primary Application
CSSP-AQFDN120	VX5B3D	MIPI-4[a]	LVDS-2[b]	1920 x 1200	Smartphones and tablet computers
CSSP-ADFDN120	VX5A1D	RGB	LVDS-1[c]	1280 x 800	Smartphones and tablet computers
CSSP-ARFDN120	VX5A3D	RGB	LVDS-2	1920 x 1200	Smartphones and tablet computers
CSSP-ACFDN120	VX5B1D	MIPI-2[d]	LVDS-1	1280 x 800	Smartphones and tablet computers
CSSP-AXFDN120	VX5B3A	MIPI-4	RGB	1920 x 1200	Smartphones and tablet computers
CSSP-AYFDN120	VX5B2A	MIPI-2	RGB	1366 x 768	Smartphones and tablet computers
CSSP-AZFDN120	VX5A3B	RGB	MIPI-4	1920 x 1200	Smartphones and tablet computers
CSSP-BAFDN120	VX5A2B	RGB	MIPI-2	1366 x 768	Smartphones and tablet computers

a. MIPI-4: Four lane MIPI interface.
b. LVDS-2: Dual link LVDS interface (eight data differential pairs and two clock differential pairs).
c. LVDS-1: Single link LVDS interface (four data differential pairs and one clock differential pair).
d. MIPI-2: Two lane MIPI interface.

Data Paths

VX5B3D — MIPI-4 to LVDS-2

Figure 1: VX5B3D Architecture



Use Case

Data path input and outputs are:

- Input – MIPI 4-lane
- Output – LVDS dual link (four data differential pairs and one clock differential pair)

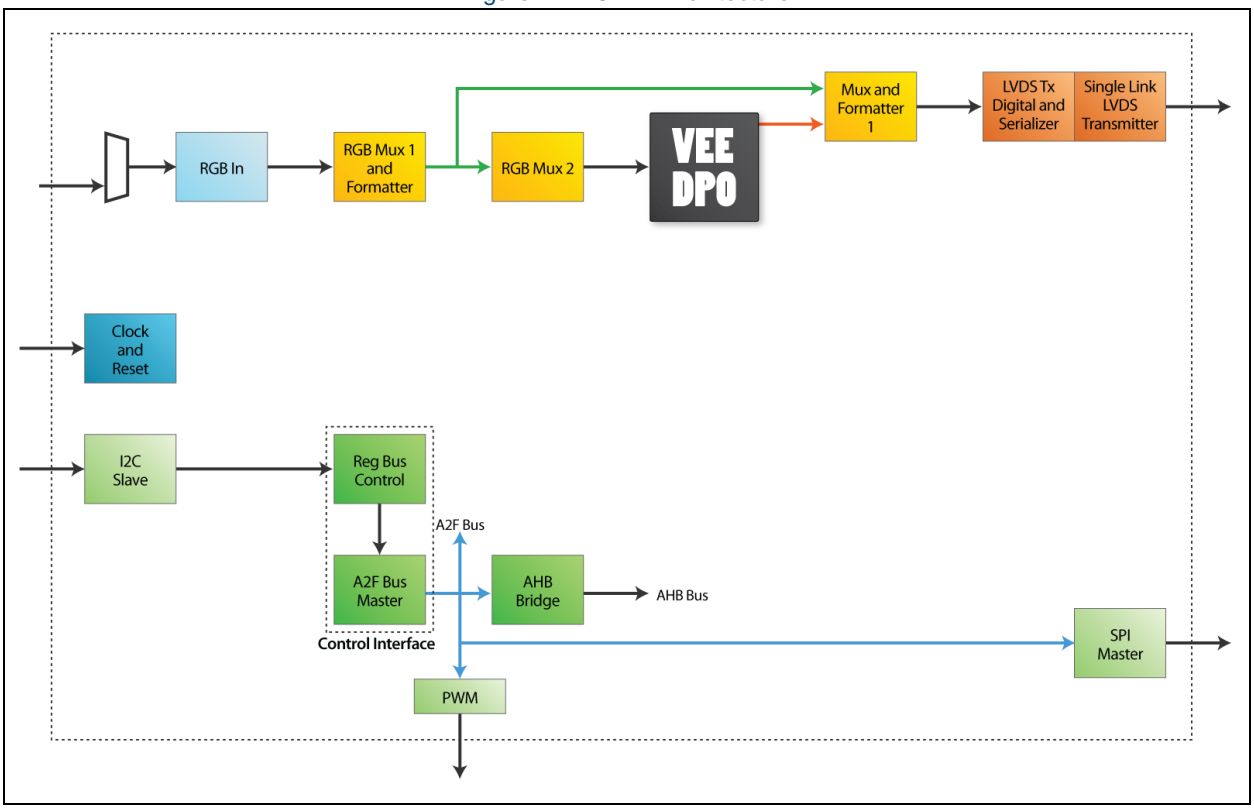
Control path input and outputs are:

- Input – I^2C
- Output – SPI

Maximum resolution is WUXGA (1920 x 1200) at 24 bpp at 60 fps. The speed is limited by LVDS bandwidth.

VX5A1D — RGB to LVDS-1

Figure 2: VX5A1D Architecture



Use Case

Data path input and outputs are:

- Input – RGB
- Output – LVDS single link (four data differential pairs and one clock differential pair)

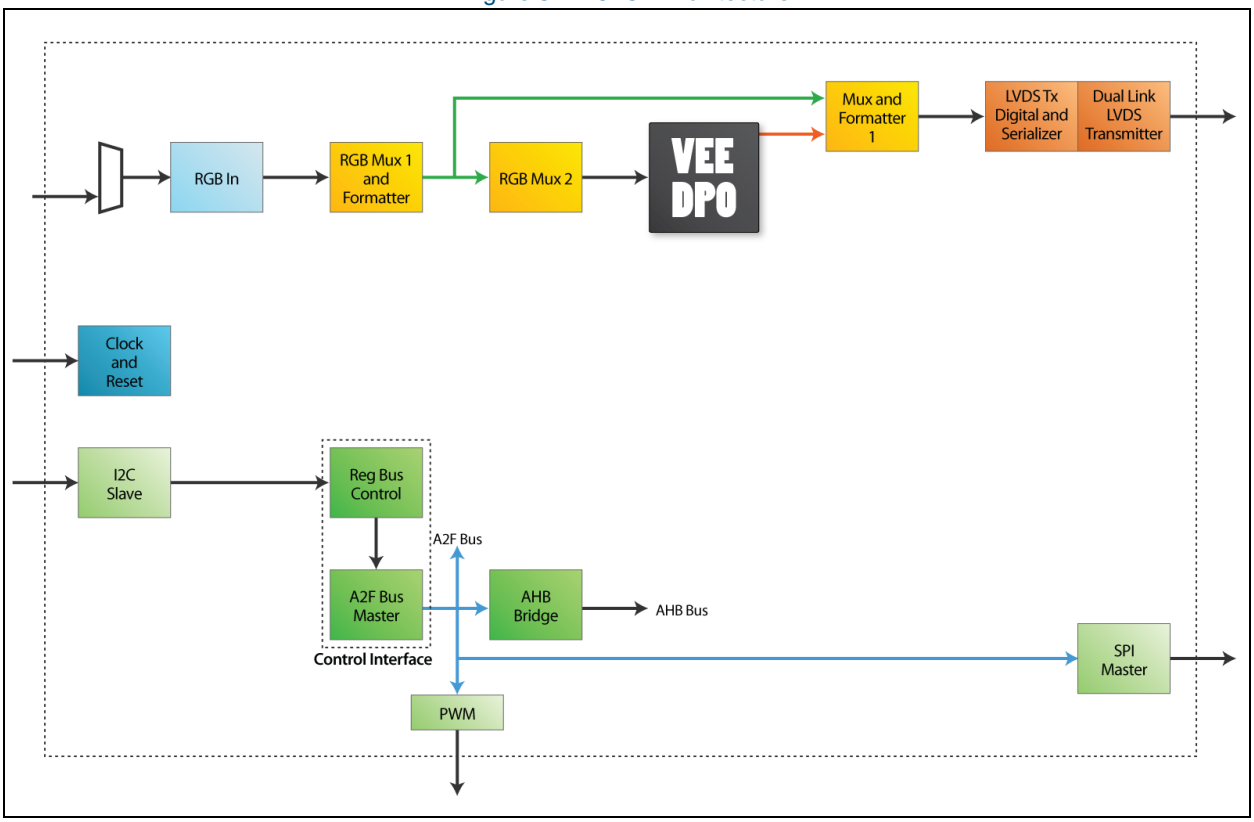
Control path input and outputs are:

- Input – I^2C
- Output – SPI

Maximum resolution is 1280 x 800 at 24 bpp at 60 fps. The speed is limited by LVDS bandwidth, and resolution is dependent on display blanking and pixel clock.

VX5A3D — RGB to LVDS-2

Figure 3: VX5A3D Architecture



Use Case

Data path input and outputs are:

- Input – RGB
- Output – LVDS dual link (eight data differential pairs and two clock differential pairs)

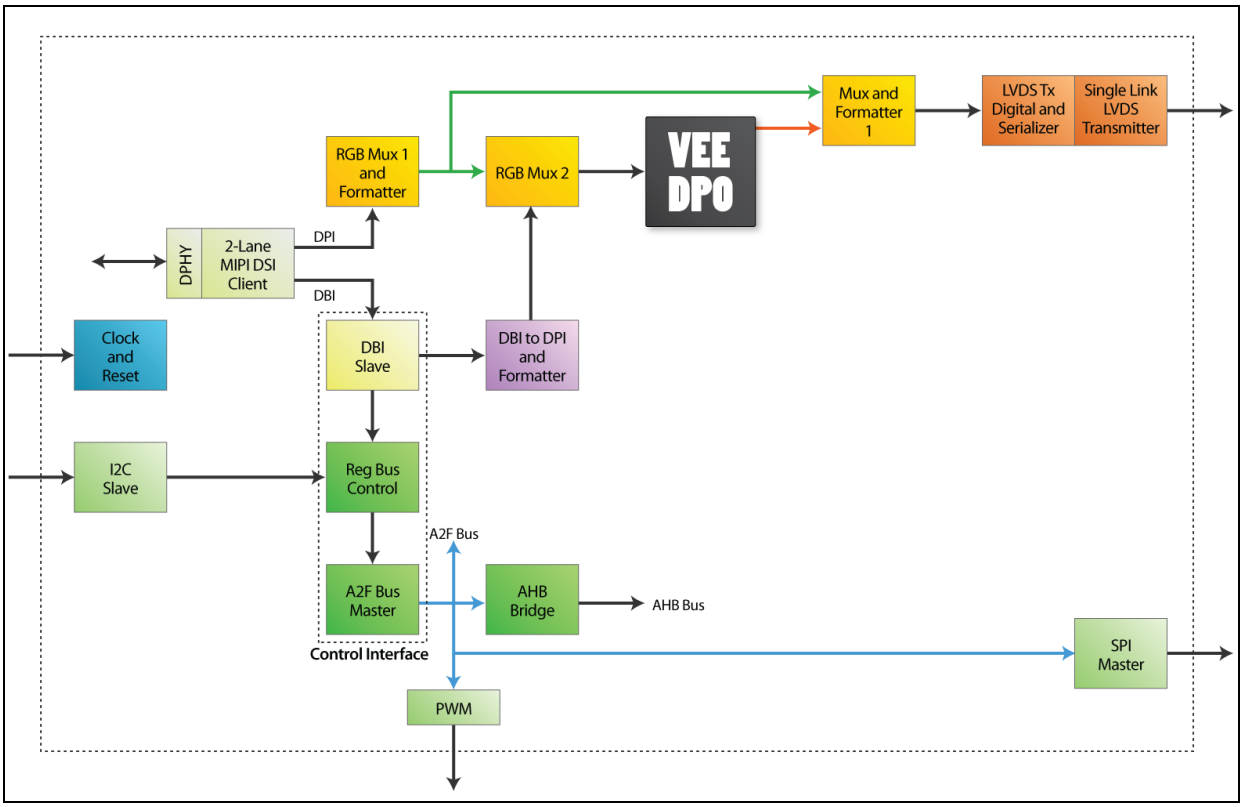
Control path input and outputs are:

- Input – I^2C
- Output – SPI

Maximum resolution is 1920 x 1200 at 24 bpp at 60 fps. The speed is limited by LVDS bandwidth.

VX5B1D — MIPI-2 to LVDS-1

Figure 4: VX5B1D Architecture



Use Case

Data path input and outputs are:

- Input – MIPI 2-lane
- Output – LVDS single link (four data differential pairs and one clock differential pair)

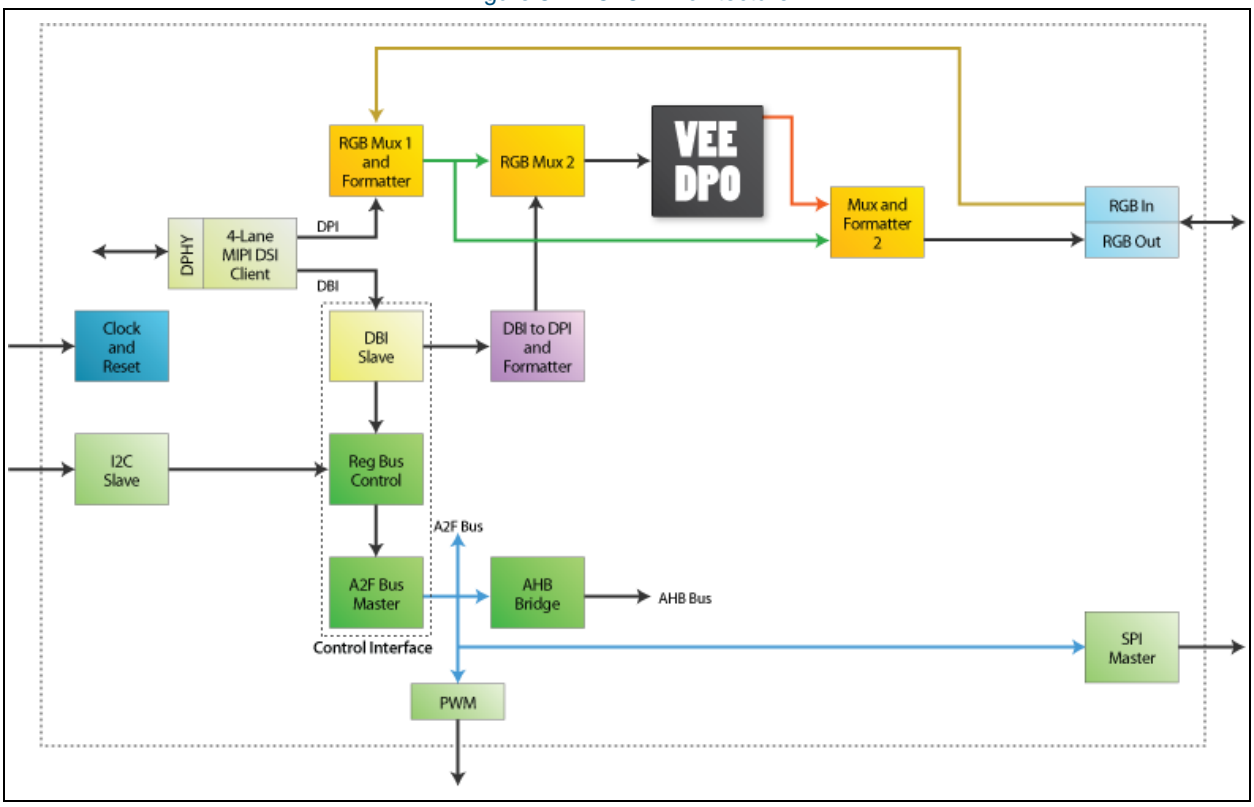
Control path input and outputs are:

- Input – I^2C and/or MIPI display bus interface (DBI)
- Output – SPI

Maximum resolution is 1280 x 800 at 24 bpp at 60 fps. The speed is limited by LVDS bandwidth, and resolution is dependent on display blanking and pixel clock.

VX5B3A — MIPI-4 to RGB

Figure 5: VX5B3A Architecture



Use Case

Data path input and outputs are:

- Input – MIPI 4-lane
- Output – RGB

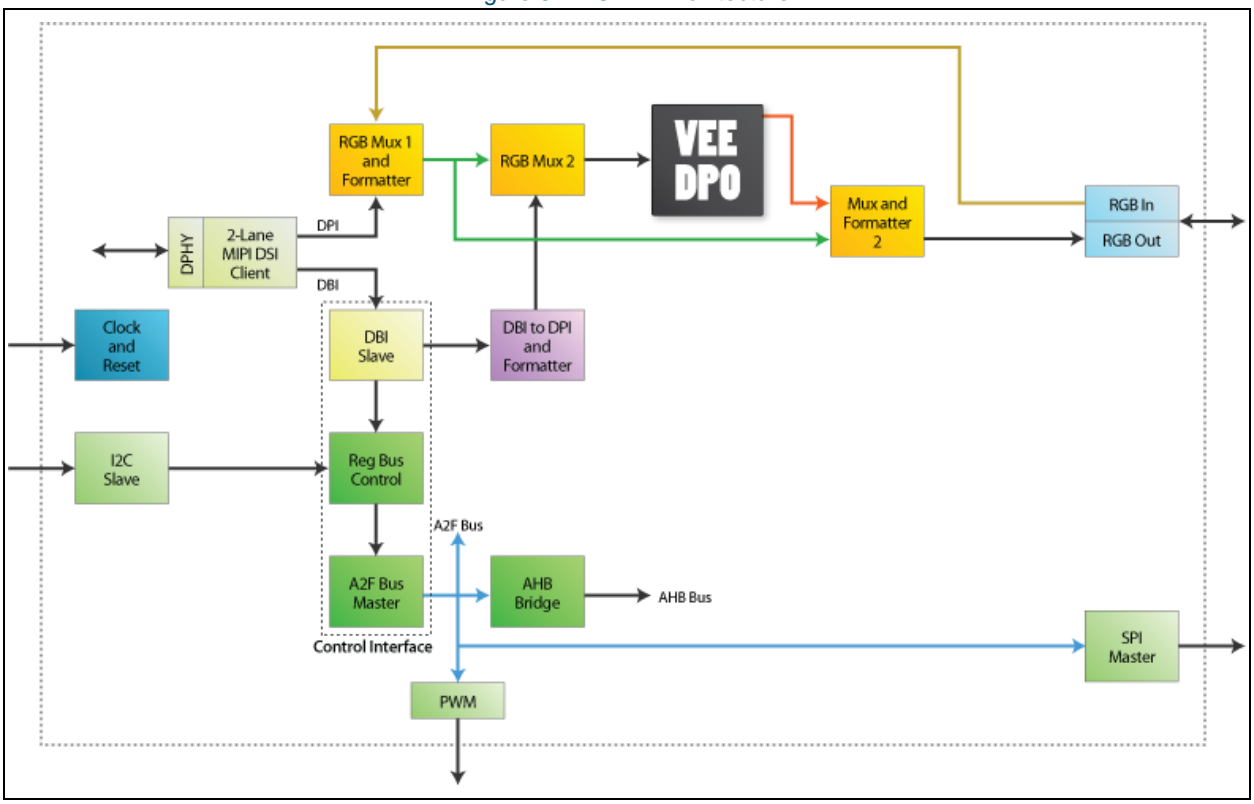
Control path input and outputs are:

- Input – I^2C and/or MIPI display bus interface (DBI)
- Output – SPI

Maximum resolution is 1920 x 1200 at 24 bpp at 60 fps. The speed is limited by MIPI bandwidth.

VX5B2A — MIPI-2 to RGB

Figure 6: VX5B2A Architecture



Use Case

Data path input and outputs are:

- Input – MIPI 2-lane
- Output – RGB

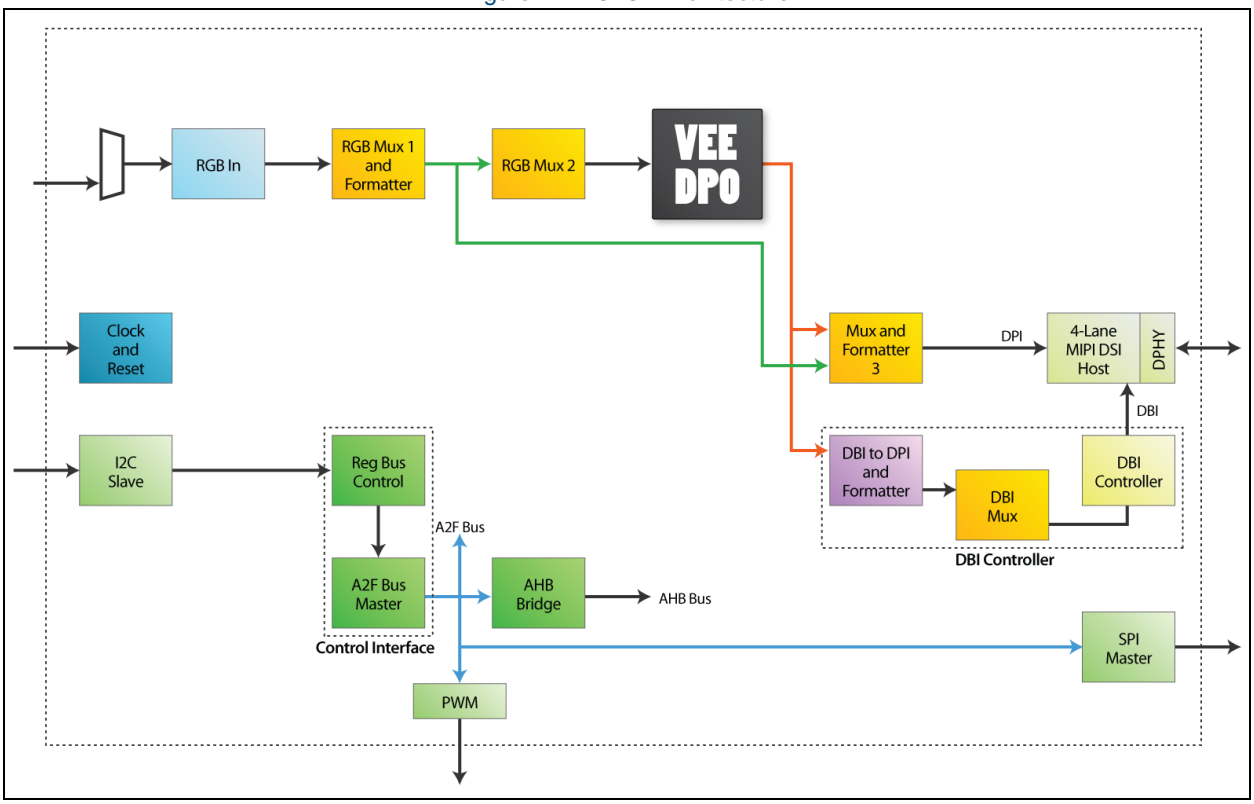
Control path input and outputs are:

- Input – I^2C and/or MIPI DBI)
- Output – SPI

Maximum resolution is 1366 x 768 at 24 bpp at 60 fps. The speed is limited by MIPI bandwidth.

VX5A3B — RGB to MIPI-4

Figure 7: VX5A3B Architecture



Use Case

Data path input and outputs are:

- Input – RGB
- Output – MIPI 4-lane

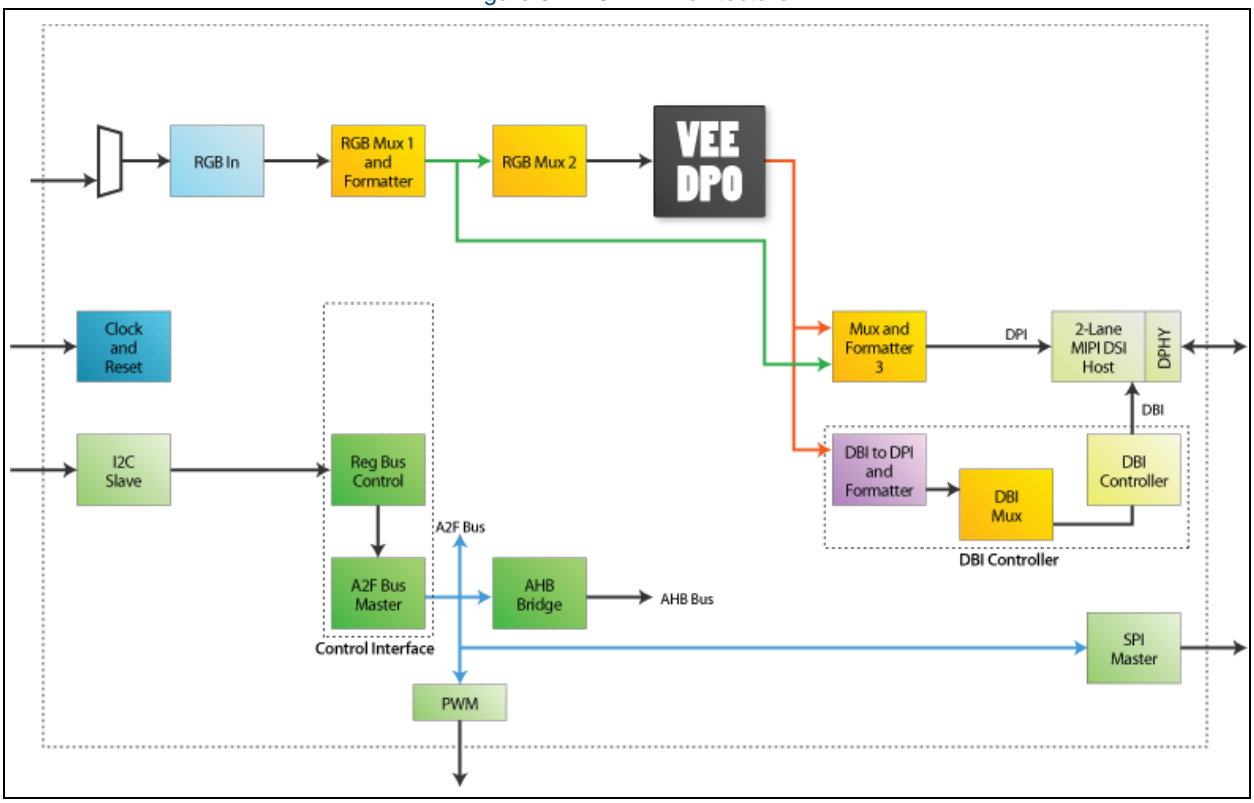
Control path input and outputs are:

- Input – I^2C
- Output – SPI and/or MIPI DBI

Maximum resolution is 1920 x 1200 at 24 bpp at 60 fps. The speed is limited by MIPI bandwidth.

VX5A2B — RGB to MIPI-2

Figure 8: VX5A2B Architecture



Use Case

Data path input and outputs are:

- Input – RGB
- Output – MIPI 2-lane

Control path input and outputs are:

- Input – I^2C
- Output – SPI and/or MIPI DBI

Maximum resolution is 1366 x 768 at 24 bpp at 60 fps. The speed is limited by MIPI bandwidth.

Power Consumption

Table 2 and **Table 3** shows the power consumption in various operating modes.

Table 2: VX5Axx Power Consumption (mW) at 60 fps[a]

Resolution	Display Width (pixels)	Display Height (pixels)	VX5A2B[a]		VX5A3B[b]		VX5A1D		VX5A3D	
			18 bpp	24 bpp	18 bpp	24 bpp	18 bpp	24 bpp	18 bpp	24 bpp
QVGA	320	240	28.1	28.1	32.8	32.9	71.42	71.4	148.4	148.9
VGA	640	480	32.2	33.1	36.9	37.0	72.6	72.6	150.9	151.4
WVGA	854	480	34.6	35.7	38.5	38.6	73.1	73.1	151.8	152.3
PAL	768	576	35.9	37.0	39.1	39.3	73.3	73.3	152.3	152.8
SVGA	800	600	36.4	38.0	39.8	40.1	73.5	73.5	152.7	153.2
XGA	1,024	768	42.9	46.2	45.6	46.9	75.0	75.0	155.9	156.4
HD 720	1,280	720	45.5	49.4	48.0	49.3	75.6	75.6	157.1	157.6
WXGA	1,366	768	48.4	52.6	50.6	52.0	-	-	158.3	158.8
SXGA	1,280	960	52.8	-	54.7	56.6	-	-	160.8	161.4
SXGA	1,280	1,024	54.8	-	56.2	58.3	-	-	161.7	162.2
SXGA+	1,400	1,050	57.5	-	58.7	60.6	-	-	162.9	163.4
UXGA	1,600	1,200	-	-	73.9	76.8	-	-	185.5	186.0
HD 1080	1,920	1,080	-	-	76.8	79.5	-	-	186.7	187.3
WUXGA	1,920	1,200	-	-	82.0	84.8	-	-	189.7	190.2

a. MIPI DBI command mode is limited to FWVGA (854x480) maximum.
b. Power measurement is shown with a 3.3 V RGB I/O. If a 1.8 V RGB I/O is used, power consumption drops approximately 5 mW at 1080P (1920x1080) resolution.

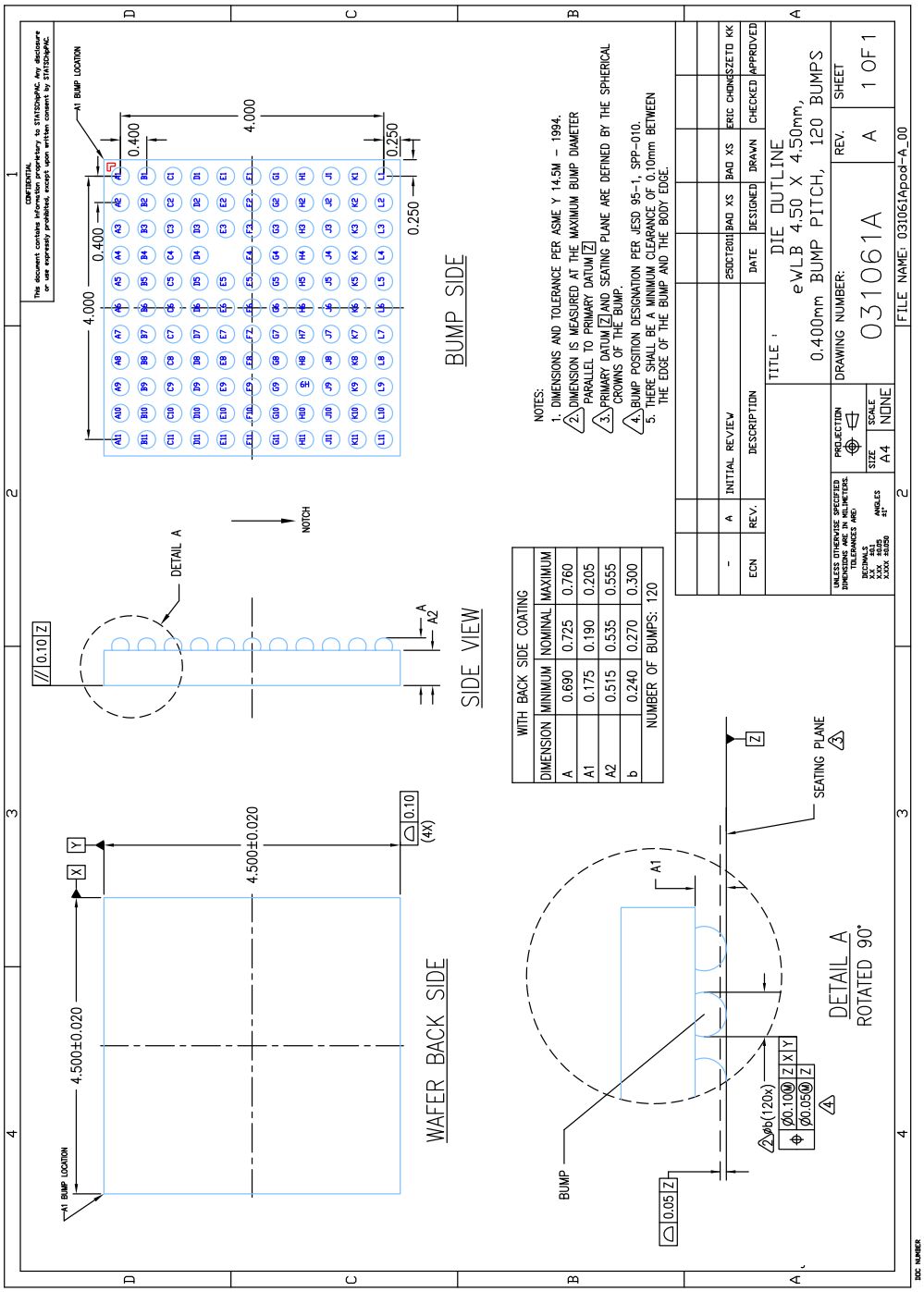
Table 3: VX5Bxx Power Consumption (mW) at 60 fps[a]

Resolution	Display Width (pixels)	Display Height (pixels)	VX5B2A		VX5B3A		VX5B1D		VX5B3D	
			18 bpp	24 bpp	18 bpp	24 bpp	18 bpp	24 bpp	18 bpp	24 bpp
QVGA	320	240	20.8	24.0	20.6	23.8	72.1	72.4	144.6	146.2
VGA	640	480	29.4	34.1	29.1	33.8	75.2	75.7	148.5	150.2
WVGA	854	480	33.0	38.2	32.7	37.9	76.6	77.1	151.7	154.0
PAL	768	576	34.8	40.3	34.5	39.9	77.3	77.9	151.0	152.7
SVGA	800	600	36.0	41.9	35.6	41.4	77.8	78.3	151.6	153.3
XGA	1,024	768	47.2	54.9	46.8	54.3	82.1	82.6	156.8	158.5
HD 720	1,280	720	51.4	59.9	50.9	59.3	83.7	84.3	158.6	160.4
WXGA	1,366	768	55.7	64.9	55.2	64.3	-	-	160.6	162.4
SXGA	1,280	960	63.4	-	62.8	73.1	-	-	164.4	166.3
SXGA	1,280	1,024	66.5	-	65.8	76.7	-	-	165.8	167.6
SXGA+	1,400	1,050	70.5	-	69.8	81.3	-	-	167.6	169.5
UXGA	1,600	1,200	-	-	84.8	99.0	-	-	175.5	195.2
HD 1080	1,920	1,080	-	-	89.3	104.2	-	-	193.6	197.6
WUXGA	1,920	1,200	-	-	97.3	113.5	-	-	197.6	201.7

a. MIPI DBI command mode is limited to FWVGA (854x480) maximum.

Mechanical Drawing

Figure 9: VX5 Solution Platform – CSSP 120 0.4 mm Ball (4.5 mm x 4.5 mm) WLCSP Mechanical Drawing



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Revision History

Revision	Date	Originator and Comments
1.0	October 2012	Initial production release.
1.1	June 2013	Kathleen Bylsma Update contact information.
1.2	June 2013	Kathleen Bylsma Update contact information.
1.3	July 2013	Paul Karazuba and Kathleen Bylsma Update power consumption table for VX5A1D and VX5B1D.
1.4	June 2016	Brian Faith and Kathleen Bylsma Added QuickLogic Part Order Number to Table 1.

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