QuickLogic ArcticLink III GPIO Configuration

QuickLogic Application Note 107

Introduction

The QuickLogic ArcticLink III family of devices all have GPIO pins that are multi-functional. Some GPIO can be changed to different functions. Other GPIO are used to set internal configuration registers based on the input values during the power-up sequence. After powering up, these GPIO switch to the corresponding normal operation settings.

ArcticLink_III GPIO Functions

The following gives a brief summary of the various GPIO that are available in all ArcticLink III devices. As shown in **Table 1**, some GPIO have different functions during the power-up sequence. These GPIO values are latched to the ArcticLink III device during reset. At that time, the external host can drive the desired values, and then tri-states these lines after coming out of the reset state as these GPIO switch to their normal operation functions. Alternatively, the GPIO that have power-up configuration functions can be terminated externally with either a pull-up or pull-down resistor.

Table 1: ArcticLink III GPIO Configuration Summary

GPIO Number	Data Sheet Reference	Power-Up Configuration Function	Normal Operation Function
GPIO(0)	PWM_1/GPIO<0>	SYS_CLK input frequency range	PWM 1 output
GPIO(1)	PWM_2/GPIO<1>	MIPI LP clock divider value	PWM 2 output
GPIO(2)	SCLK/GPIO<2>	I^2C Slave Address bit 0	SPI SCLK
GPIO(3)	SDO/GPIO<3>	I^2C Slave Address bit 1	SPI SDO
GPIO(4)	I2C_SDA/GPIO<4>	unused	I^2C SDA
GPIO(5)	I2C_SCL/GPIO<5>	unused	I^2C SCL
GPIO(6)	SDI/GPIO<6>	unused	SPI SDI
GPIO(7)	SS/GPIO<7>	unused	SPI SS
GPIO(8)	GPIO<8>	unused	unused

GPIO Power-Up Configuration Functions

The ArcticLink III GPIOs 0, 1, 2, and 3 are used as configuration pins during power-up. Depending upon whether there is an external pull-up or pull-down resistor, the corresponding setting is assigned. The following are more in-depth details about the functional behavior of these ArcticLink III GPIO and how to configure them.

- **GPIO(0)**:
  - When GPIO(0) has an external pull-down to ground, it indicates that the SYS_CLK input frequency is between 9 MHz and 20 MHz.
- **GPIO(1):**

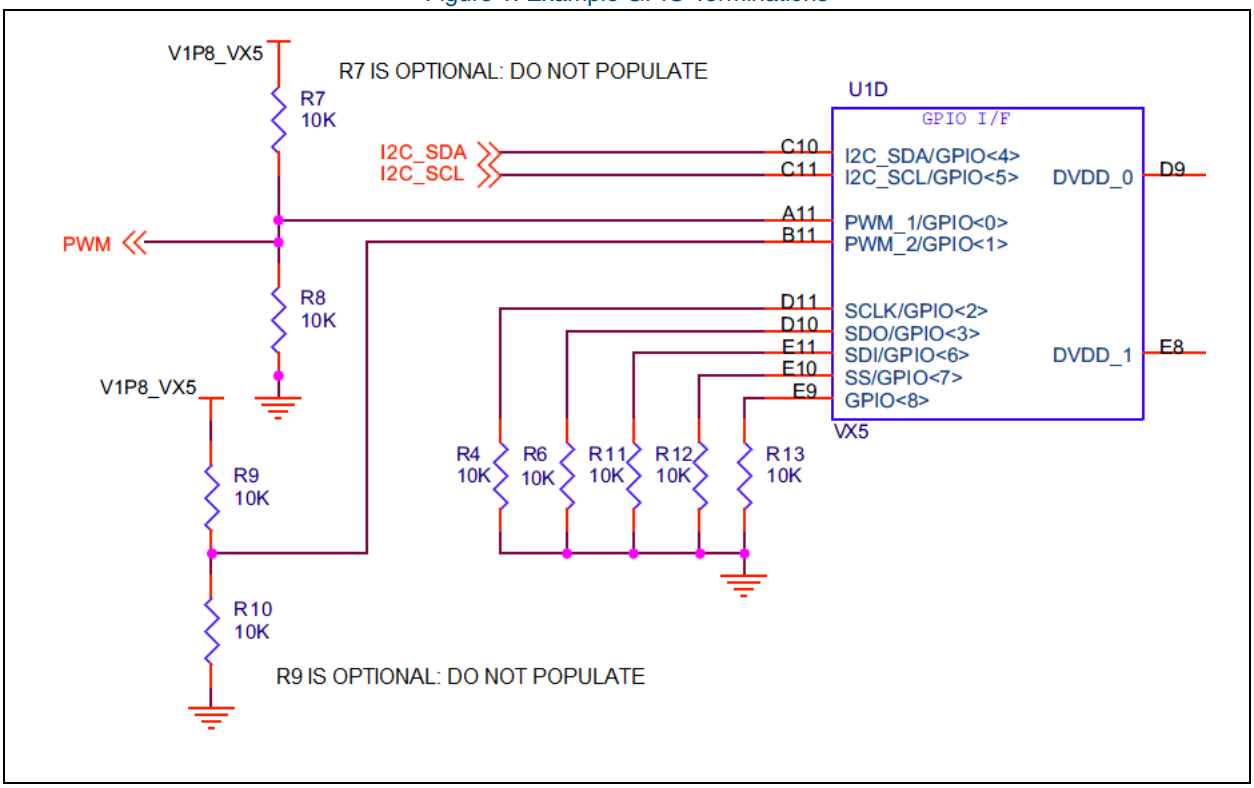
  GPIO(1) configures the MIPI Low Power (LP) Clock settings of the MIPI Client interface to the ArcticLink III. As per the MIPI specification, the host processor is responsible for controlling its own clock frequency to match the MIPI client peripheral. The host processor LP clock frequency must be in the range of 67% to 150% of the client LP clock frequency. By default, the MIPI LP clock of the ArcticLink III is the same frequency as the SYS_CLK input. If the SYS_CLK needs to be divided by two to be within 67% to 150% of the processor LP clock, then GPIO(1) should have an external pull-up resistor populated. In summary:
  - When GPIO(1) has an external pull-down to ground, it indicates that the SYS_CLK input frequency is within 67% to 150% of the host MIPI LP clock.
  - When GPIO(1) has an external pull-up to DVDD_0, it indicates that the SYS_CLK input frequency divided by two is within 67% to 150% of the host MIPI LP clock.
- **GPIO(2):**
  - When GPIO(2) has an external pull-down to ground, it sets the I^2C Slave Address bit 0 to '0'.
  - When GPIO(2) has an external pull-up to DVDD_1, it sets the I^2C Slave Address bit 0 to '1'.
- **GPIO(3):**
  - When GPIO(3) has an external pull-down to ground, it sets the I^2C Slave Address bit 1 to '0'.
  - When GPIO(3) has an external pull-up to DVDD_1, it sets the I^2C Slave Address bit 1 to '1'.

  As an example, if GPIO(2) is pulled down, and GPIO(3) is pulled up, the resulting 7-bit I^2C Slave Address would be "1100110", which is 0x66 in hexadecimal.

External Terminations

The following **Figure 2**, shows an example schematic of how to configure the various external termination resistors to the GPIO. If the input frequency of the SYS_CLK signal and LP clock of the MIPI Host is unknown, optional pull-up resistor locations can be designed for the board. It is important to note, that if an ArcticLink III device has either a MIPI Host or MIPI Client, GPIO(0) must be pulled-down since SYS_CLK must be between 9 MHz to 20 MHz. Conversely, if there is no MIPI Host or MIPI Client, GPIO(1) can be either a pull-up or a pull-down.

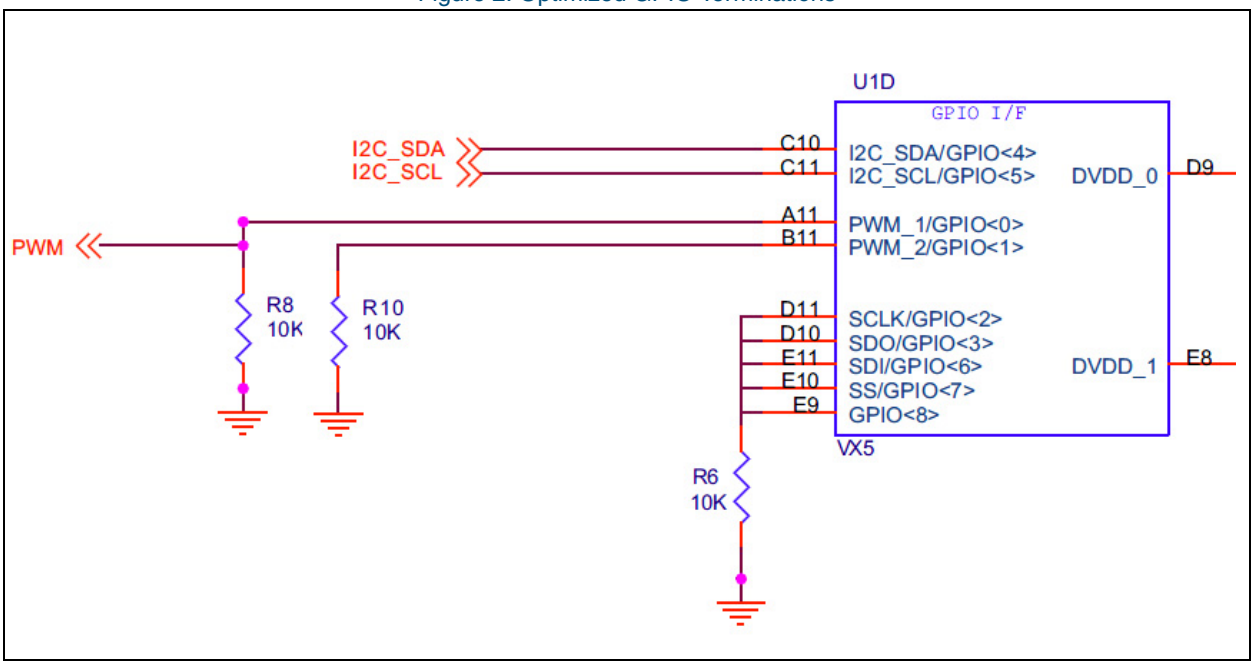
Figure 1: Example GPIO Terminations



If the 7-bit I^2C Slave Address of the ArcticLink III can be set to 0x64, GPIO(2), GPIO(3), GPIO(6), GPIO(7), and GPIO(8) can be pulled down using the same termination resistor. This can help to decrease the number of resistors required for the design.

Generally speaking, unused inputs should always be either pulled up or pulled down. This is because the output of the I/O buffers can couple with the input of the same buffer and result in a high speed oscillation. This produces noise and, potentially, higher current draw than is wanted. Therefore, even though GPIO(4) through GPIO(8) do not have a power-up setting, it is still good engineering practice to terminate them. **Figure 2**, below shows a more optimized configuration for a board that has a SYS_CLK frequency between 9 MHz and 20 MHz, a MIPI LP clock equal to the SYS_CLK, and with a 7-bit I^2C Slave Address of 0x64.

Figure 2: Optimized GPIO Terminations



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Revision History

Revision	Date	Originator and Comments
A	June 2013	Jason Lew and Kathleen Bylsma

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