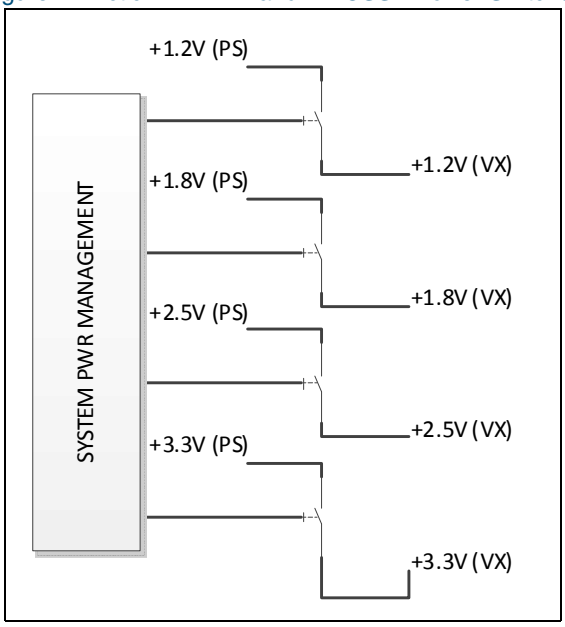
QuickLogic® ArcticLink® III VX and BX CSSPs – Power Switch Options

QuickLogic White Paper

Introduction

To provide optimum power management in a mobile system, the design must provide the ability to control individual device power supplies. This type of control logic is often implemented using power switches. As shown in **Figure 1**, QuickLogic ArcticLink III VX and BX Customer Specific Standard Product (CSSP) reference designs use four load switches, such as the Fairchild Semiconductor® FPF1208UCX, to control the required +1.2V, +1.8V, +2.5V and +3.3V power supplies (device-dependant—not all devices require these signals). While the FPF1208UCX has the advantage of integrating all required components into a single package with a very small PCB foot-print, system cost constraints can require a different power switch solution.

Figure 1: ArcticLink III VX and BX CSSP Power Switches



This document provides an alternate power switch implementation using readily-available P-Channel metal–oxide–semiconductor field-effect transistors (MOSFETs), and describes the advantages and disadvantages for this method. The circuit shown in **Figure 2** serves as an example design. The designer must carefully review system requirements to choose the appropriate implementation.

NOTE: The implementation in this document applies to the ArcticLink III VX and BX devices only. For other devices, please consult the appropriate device specification, application requirements and system constraints.

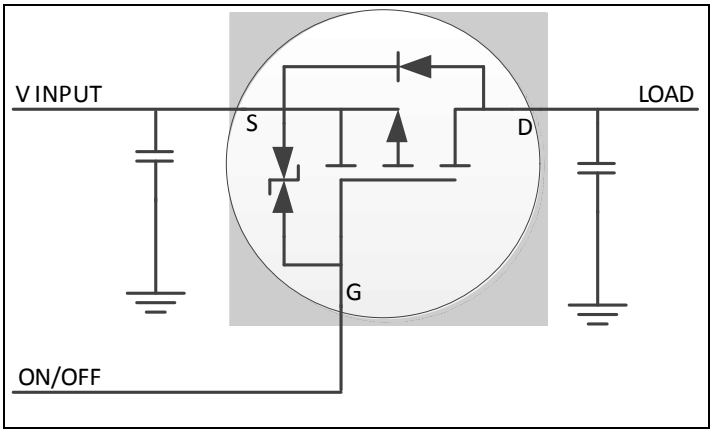
Implementation with P-Channel MOSFET

Example Implementation

In **Figure 2**, a P-Channel MOSFET is used to perform the power switch function. A 2.2 µF is placed at the input and a 0.1 µF capacitor is placed at the output of the switch. The capacitors provide storage and also act as a filter for noise on the power line.

NOTE: The size of the capacitor is scaled based on the in-rush current expected. Insufficient capacitance can result in a significant, temporary voltage drop on the supply side of the gate when the switch is turned on.

Figure 2: Power Switch using a P-Channel MOSFET



With this implementation, a MOSFET switch is connected between the positive power rail (high side) and the load. In a P-Channel device, the flow of drain current is in a negative direction so a negative gate-source voltage is applied to switch on the MOSFET. When the voltage on the gate approaches threshold voltage, the switch turns off. This switching behavior enables the gate terminal to be driven by a standard digital logic gate.

This circuit is useful in applications requiring low supply currents and fast turn-on times.

Device Selection

Given the maturity and availability of MOSFETs, selecting the device for a power switching application can be a simple process. However, there are a few parameters that need special consideration.

The driving factors for device selection are:

- Amount of current the load requires
- Power loss in the switch
- Level of switching voltage

The trade-offs between these parameters affects the overall design cost and the PCB size. In general, devices that provide low power loss and high supply current are costly and require larger package sizes.

Device Parameters

The three most important parameters to look for when selecting the MOSFET to use as a switch are:

- **Maximum drain source voltage (breakdown voltage):** The breakdown voltage must be higher than the voltage the application requires.
- **Maximum drain current:** The maximum drain current must be greater than what is needed by the load.
- **On-resistance:** The on-resistance must be as low as possible compared to the resistance of the load.

Table 1 describes additional important parameters.

Table 1: MOSFET Switch Parameters

Parameter	Description
V_{DSS}	**Drain source voltage:** This is the rating of the maximum drain source voltage without causing the device to breakdown. It is often referred to as the maximum voltage between drain and source before damaging the FET.
V_{GS}	**Gate source voltage:** This is the gate source voltage at which drain current begins to flow, or stops flowing when switching off the MOSFET. Test conditions (i.e., drain current, drain source voltage, and junction temperature) are also specified. All MOS-gated devices exhibit variations in threshold voltage between devices, which is normal. Therefore, a range in $V_{GS(th)}$ is specified, with the minimum and maximum representing the edges of the $V_{GS(th)}$ distribution.
I_D	**Continuous drain current:** This is the maximum continuous drain current the device can handle. Depending on the operating environment and load current requirements, it is recommended to use, at minimum, a 20% overhead allowance for current.
P_D	**Total power dissipation:** This is the rating of the maximum power that the device can dissipate and is based on the maximum junction temperature and the thermal resistance of the case to temperature changes.
$R_{DS(ON)}$	**On resistance:** This is the drain source resistance at a specified drain current (usually half the ID current) and gate source voltage (usually 10 V). At 25°C unless otherwise specified. **Derating factor:** This is the maximum power dissipation is decreased by this amount if the case temperature is more than the reference temperature,
$R_{\theta JC}$	**Junction to case thermal resistance:** This is the thermal resistance from the junction of the die to the outside of the device case. Heat is the result of power lost in the device itself, and thermal resistance relates how hot the die gets relative to the case based on this power loss.
$t_{d(on)}$	**Turn-on delay time:** This is the time from when the gate source voltage rises past 10% of the gate drive voltage to when the drain current rises past 10% of the specified current.
$t_{d(off)}$	**Turn-off delay time:** This is the time from when the gate source voltage drops below 90% of the gate drive voltage to when the drain current drops below 90% of the specified current. This gives an indication of the delay before current begins to transition in the load.
t_r	**Rise time:** This is the time between the drain current rising from 10% to 90%, start to stop of the specified current.
t_f	**Fall time:** This is the time between the drain current falling from 90% to 10%, start to stop of the specified current.

P-Channel MOSFET Comparison Examples

Table 2 presents a few examples of P-Channel MOSFETs which can be useful in ArcticLink III BX and VX CSSP power rails switches. Since each system design is unique, the device selection must be done with consideration for the specific application. Device and device manufacturer selection is a complex issue and it is not addressed here. The list is provided as examples for further research.

Table 2: P-Channel MOSFETs

Device	Cost per Unit ($)	Size (mm)	Package	Manufacturer
FPF1208UCX[a]	0.70	0.76 x 0.76	WLCSP	Fairchild®
BSS84-7-F	0.39	3.0 x 3.0	SOT23-3	Diodes Incorporated®
DMG1017T-7	0.31	1.70 x 1.70	SOT523-3	Diodes Incorporated
Si2301CDS	0.48	2.80 x 2.81	SOT23	Vishay®
Si2315BDS	0.60	2.45 x 2.69	SOT23	Vishay
FDY102PZ	0.46	1.70 x 1.70	SOT523-F	Fairchild

a. The FPF1208UCX is the current recommended device for ArcticLink III BX and VX applications because it has the smallest PCB footprint.

See the QuickLogic *ArcticLink III VX and BX CSSPs – PCB Layout Guidelines, Application Note 97* for an example of the trade-off between cost, PCB foot-print and device specification.

Contact Information

Phone: (408) 990-4000 (US)
(647) 367-1014 (Canada)
+(44) 1932-21-3160 (Europe)
+(886) 26-603-8948 (Taiwan)
+(86) 21-5179-8474 (China)
E-mail: info@quicklogic.com
Sales: America-sales@quicklogic.com
Europe-sales@quicklogic.com
Asia-sales@quicklogic.com
Japan-sales@quicklogic.com
Support: www.quicklogic.com/support
Internet: www.quicklogic.com

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Revision	Date	Originator and Comments
A	July 2012	Anthony Le and Kathleen Bylsma

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