QuickLogic® ArcticLink® III VX and BX CSSPs – PCB Layout Guidelines

QuickLogic Application Note 97

Introduction

This document provides guidelines for designing a printed circuit board (PCB) that includes the QuickLogic ArcticLink III VX and/or BX Customer Specific Standard Products. (CSSPs).

When designing a PCB with an ArcticLink III VX/BX CSSP, extreme care must be given to the following areas:

- Device interface signals: clock routing and other data lines that run between devices on the PCB.
- Power going into the device from the connector: the power lines to the device must be filtered to pass only low frequency signals of less than 100 kHz. The ground signals must have returned current during data transmission.
- External clock circuit.
- Differential pair signals: impedance and length matching.

This document is divided into two sections: a generic layout and a specific layout for ArcticLink III VX/BX CSSPs.

Generic Layout Guidelines

The following generic guidelines are from QuickLogic for a board design that contains an ArcticLink III VX/BX CSSP. PCB designers should consult internal PCB design rules and recommendations, as well as other device manufacturers, to produce a working PCB.

Important PCB design elements include:

- Type of circuit (analog, digital, etc.)
- Board size
- Number of layers
- Pad stack sizes
- Hole sizes
- Layer thickness
- Board thickness
- External connections
- Mounting holes
- Supply and ground layer thickness
- Component details with specifications

Important design rules are:

- Power distribution and coupling
- Critical signal paths
- IR [Current (I) x Resistance (R)] drops in signal and power traces
- Impedance control
- Pad/land geometries
- Trace width/spacings
- Plated/unplated hole sizes
- Part placement constraints
- Layer assignments and routing constraints
- Heat-removal paths
- Test requirements

Partitioning

The following guidelines are recommended for system partitioning:

- Divide the system into subsystems for placement. The division is used for layout partitioning of circuitries. Group components belonging to a functional block together.
- Isolate sensitive circuits (such as clocks and analog supplies) from noisy sources (such as high transition signals and power regulators).
- Separate analog power supplies from digital power supplies.

Placement

A system with an ArcticLink III VX/BX CSSP is comprised of a set of interacting elements responding to inputs to produce outputs. Good placement for logical data flow is important to keep the number of layers to a minimum.

The following guidelines are recommended for placement of components:

- For highly-sensitive circuits, place the critical components first to produce minimum trace-length.
- For less-critical circuits, arrange the components in the order of the signal flow to minimize the overall connection length.
- For components that have many connecting points, place these components first and group the remaining ones around them.
- For components with a fixed position (such as connectors), place these components first followed by components that are connected to the fixed components.

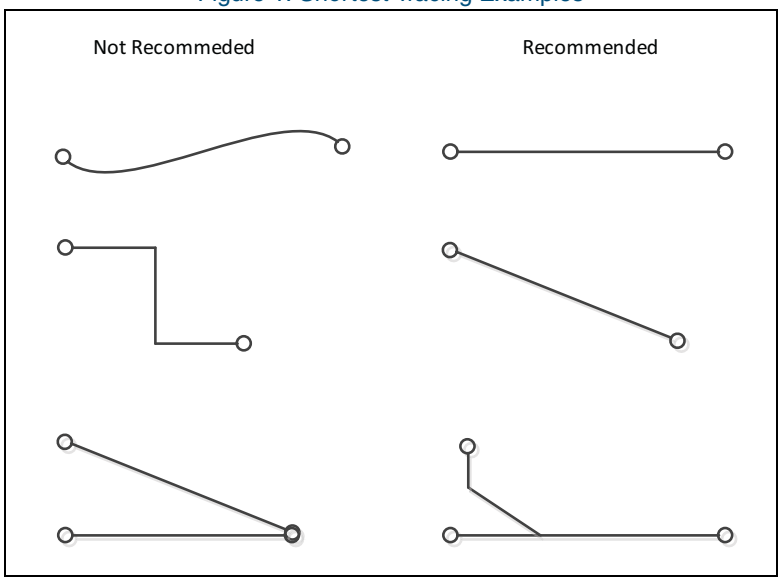
- Place the larger components (such as main devices) first. Place the smaller components (such as capacitors and resistors) between the larger components.
- Place components in rows or columns for good viewing.
- Place decoupling capacitors as close as possible (preferably adjacent) to the power pins of the device for maximum effectiveness.

Routing

The following guidelines are recommended for routing:

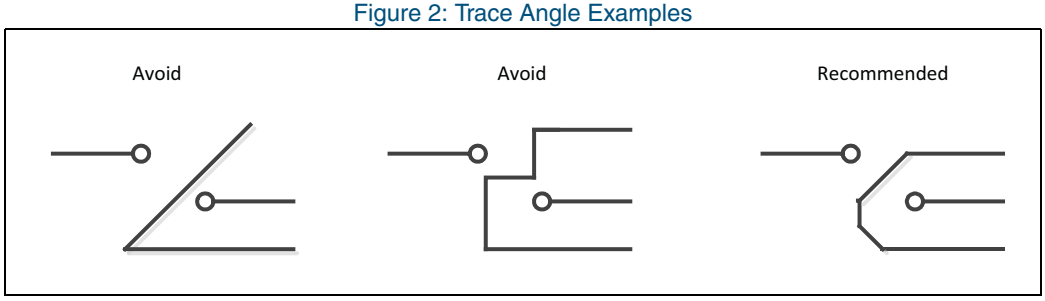
- Select the shortest interconnection length, especially for high frequency circuits (see **Figure 1**).

Figure 1: Shortest Tracing Examples



- Place traces with a minimum angle of 60 degrees (see **Figure 2**).

Figure 2: Trace Angle Examples



- Place parallel traces at the same angle to ensure uniformity, and eliminate the variance in the traces spacing.
- Distribute the spacing equally when one or more traces pass between pads or other conductive areas. To obtain maximum spacing, place traces perpendicular to a narrow passage.
- Distribute traces widely over the available area to avoid issues in manufacturing (i.e., do not space parallel running traces closely).
- Avoid unwanted bunching.

- Match signal impedance for all high-speed signals.
- Ensure that power lines are as thick as possible. Check the current requirements for the line.
- Ensure that the ground traces are always two times wider than the power traces.
- Distribute the routing pattern equally between the various layers of the PCB to achieve uniform plating in the manufacturing process.
- Route adjacent signal layers orthogonally to each other.
- Place ground or power planes to isolate signal layers when possible.
- Route traces directly to a connector pad without line branching to prevent reflections and impedance changes.
- Use curves or two 45° turns to avoid minor line reflections.
- Avoid line-width changes that can affect trace impedance.
- Make pads with soldered signal traces tear-dropped at the pad junction.

Power

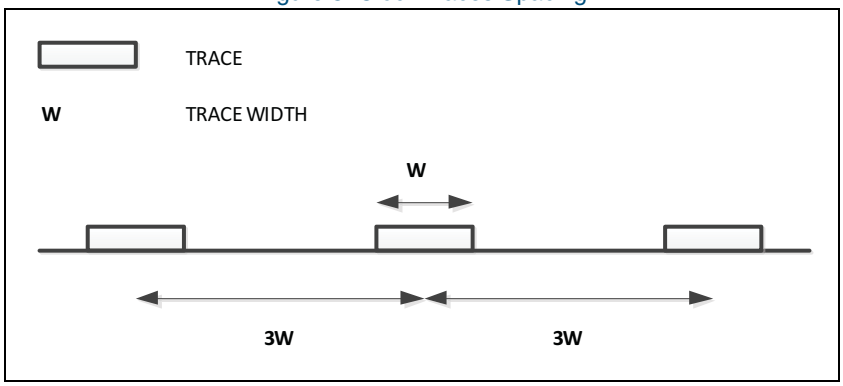
Switching power regulators are noisy and can cause noise-coupling issues if placed close to sensitive areas on the PCB. Keep these circuits away from the sensitive traces, clock circuits and connectors.

Clock Routing

The following guidelines are recommended for clock routing:

- Use series terminator resistors to eliminate reflections. Obtain the final value by looking at the waveform using a high-speed oscilloscope to obtain minimum distortion on the signal.
- Use the 3W spacing rule when routing clock traces from one device to another to minimize cross-talk (see **Figure 3**).

Figure 3: Clock Traces Spacing



- Do not use 90° angles for bending.
- Include guard traces (ground) to surround the clock signal if possible.
- Place clock routing on an internal layer without stubs.

High-Speed Differential Pair

The following guidelines are recommended for high-speed input and output signal layout:

- For low-swing signals (<300 mV), place the CSSP as close to the driving source as possible (such as the flexible printed circuit or processor) to minimize the cross-talk, impedance mismatch, and differential noise pick-up. Keep the total trace-length <4 inches.
- Traces must always be matched lengths.
- Route the pair as close together as possible for noise rejection.
- Trace impedance must be 100 Ohm ± 10% to produce a 50 Ohm ± 10% pair.
- Signals must not have extra components to maintain signal integrity.

Vias

The following guidelines are recommended for via usage:

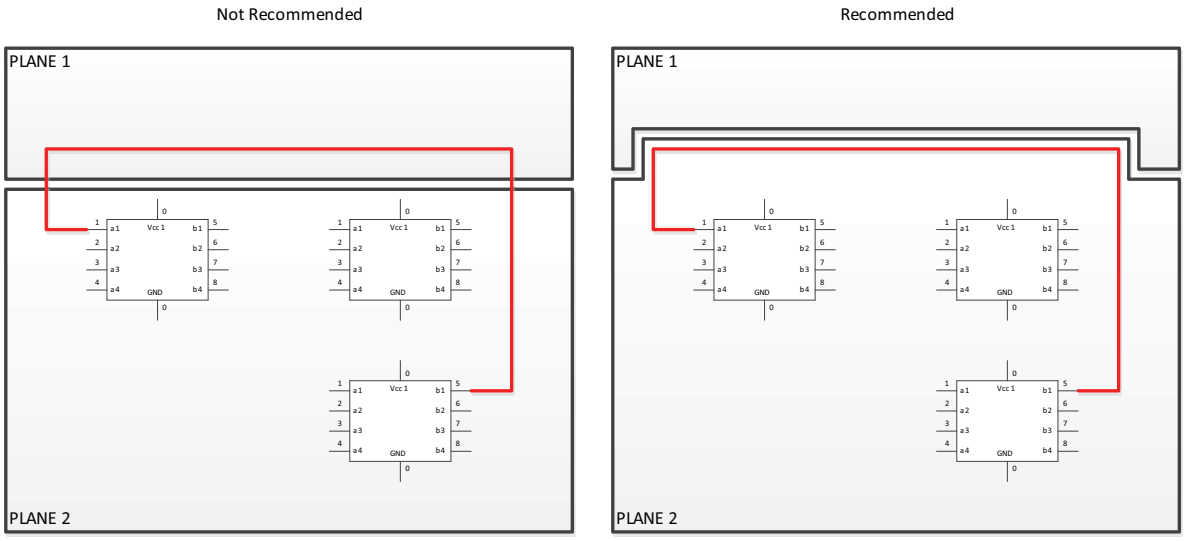
- Increase the clearance around the via to minimize capacitance.
- Minimize the number of vias per signal connection. Each via introduces discontinuities in the signal transmission line and increases the chance to pick up interference from other layers of the PCB.
- Avoid using a through-hole via as a test point if possible.

Isolations

Isolation is referred to as the separation between power and ground planes. The following guidelines are recommended for isolation:

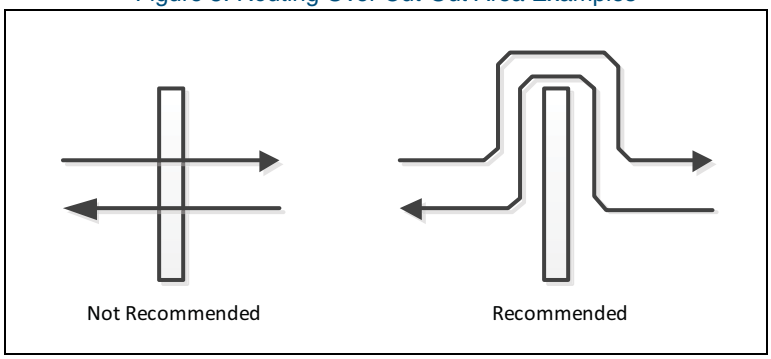
- Isolate between digital and analog power planes.
- Do not route traces across planes (see **Figure 4**). This can cause a broken RF path for the return signal, which can result in severe EMI issues. Route high-speed sensitive signals parallel to solid power or ground planes.

Figure 4: Routing Over Isolation Planes



- Fill unused areas of a layer with copper and connect to ground planes using vias.
- Do not overlap planes between layers. These overlap areas can produce unwanted capacitance that passes RF emissions between the planes.
- Do not route signals over the slot-plane (see **Figure 5**).

Figure 5: Routing Over Cut-Out Area Examples



Electrostatic Discharge (ESD)

The following guidelines are recommended for ESD:

- Provide ESD protection for PCB handling. The typical provision is an ESD strip around the board. The strip must connect to the PCB ground plane.
- Apply ESD protection to all connectors. The ground of the connector body must be connected to the PCB ground plane.

Layout Guidelines Specific to the ArcticLink III VX/BX CSSP

Critical Signals

The following guidelines are recommended for the layout of critical signals:

- Keep the ArcticLink III VX/BX CSSP reference clock circuits as close to the device as possible.
- Follow the minimum spacing rules for reset lines from adjacent signals on the same and adjacent layers.
- Keep reset lines away from noisy sources (such as long clock traces, high energy signals and fast transition edges signals).
- Keep interrupt lines away from noisy sources (such as long clock traces, high energy signals and fast transition edges signals).

Vias

Use via-in-pad for the layout of vias and device connections.

MIPI (ArcticLink III VX3, BX3, VX5Bxx, BX5Bxx, VX5xxB, BX5xxB, VX6 and BX6 only)

The following guidelines are recommended for the layout of MIPI:

- Route MIPI signals on the internal layers as much as possible.
- Keep the number of vias as close to minimum (two) as possible.
- Follow the PCB routing rules for MIPI specifications.
- Follow the recommended tolerance for length matching between pin-pair and all MIPI signals, which is ±5 mil (*see* **Table 1**).

Table 1: Recommended Tolerance for Length Matching

Pin	Signal	Pair Tolerance	Overall Tolerance
A6	MIPI RX D3 P	± 5 mil	± 5 mil
B6	MIPI RX D3 N		
A7	MIPI RX D2 P	± 5 mil	
B7	MIPI RX D2 N		
A8	MIPI RX CLK P	± 5 mil	
B8	MIPI RX CLK N		
A9	MIPI RX D1 P	± 5 mil	
B9	MIPI RX D1 N		
A10	MIPI RX D0 P	± 5 mil	
B10	MIPI RX D0 N		
F10	MIPI TX D3 P	± 5 mil	± 5 mil
F11	MIPI TX D3 N		
G10	MIPI TX D2 P	± 5 mil	
G11	MIPI TX D2 N		
H10	MIPI TX CLK P	± 5 mil	
H11	MIPI TX CLK N		
J10	MIPI TX D1 P	± 5 mil	
J11	MIPI TX D1 N		
K10	MIPI TX D0 P	± 5 mil	
K11	MIPI TX D0 N		

RGB (ArcticLink III VX5Axx, BX5Axx, VX5xxA and BX5xxA only)

The following guidelines are recommended for the layout of RGB:

- Route the RGB signals on the internal layers as much as possible.
- Keep the number of vias as close to minimum (two) as possible.
- Follow the PCB routing rules for RGB specifications.
- Comply with the target operating frequency for length matching between all RBG signals with respect to RGB_CLK (K2).

LVDS (ArcticLink III VX5xxD and BX5xxD only)

The following guidelines are recommended for the layout of LVDS:

- Route LVDS signals on the internal layers as much as possible.
- Keep the number of vias as close to minimum (two) as possible.
- Follow PCB routing rules for LVDS specifications.
- Check panel timing requirements to determine the length that matches the criteria for PCB layout.

Power

The following guidelines are recommended for the layout of power:

- Use the power island or plane as much as possible.
- If using a power trace to connect to the ArcticLink III VX/BX CSSP power pins, make the trace as wide as possible, and follow current requirements to prevent excessive IR drop.
- Since the number of capacitors for the design is at a minimum, place all of the capacitors as close to the power pins as possible.

Reducing the Number of PCB Layers

The cost-reduction requirements common to PCB design and manufacturing requires the PCB designer to look for a solution to produce PCBs at the lowest cost possible. This section discusses areas that a PCB designer needs to consider when using an ArcticLink III VX/BX CSSP in the system.

There are several factors that contribute to the cost of a bare PCB:

- Volume: the number of PCBs per run.
- PCB size: the smaller, the less costly.
- PCB material: readily available material is less expensive.
- Number of layers: thickness reduction and quicker manufacturing time.
- PCB shapes: odd shape and slots require more processes.
- Copper size and spacing: the dimension of pads and spacing demand better PCB producing equipment.
- Via: current PCB technology is capable to handle more advanced via types: blind, buried, etc. These require more manufacturing time which translates into a more costly PCB.

Work with the PCB manufacturer to understand the trade-offs between PCB cost and these factors before finalizing PCB specifications.

Device Placement

Placement of devices is critical for good flow to nets routing, thus reducing the number of layers required. The placement must follow the flow of data between components. Critical components must be placed first, followed by support components such capacitors. Less critical components are placed last.

Make sure the device orientation is correct. If the device is in the correct location, but with the wrong orientation, the intended result may not be achieved. Always choose the orientation that has the most signals flowing in the same direction. Crossing signals require multiple layers to complete routing.

Figure 6 and **Figure 7** illustrate the difference in routing based on part orientation. **Figure 6** shows the RGB bus is divided with routing going outside of an ArcticLink III VX CSSP, which makes length matching and routing easy. **Figure 7** shows a short distance for pins close to the processor, while the other RGB pins are on the other side of the package. Added length is needed for short traces to meet the length matching requirements.

Figure 6: Good Placement and Orientation Example

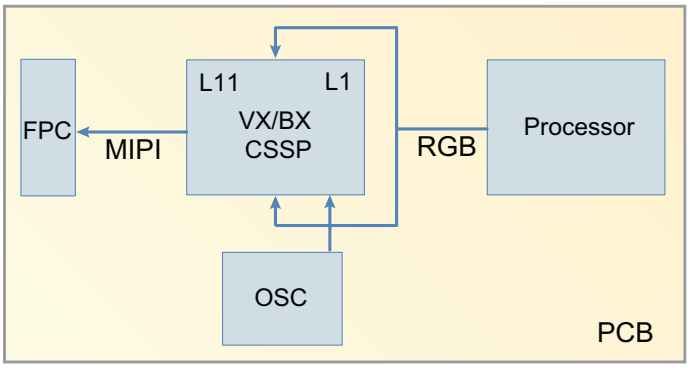
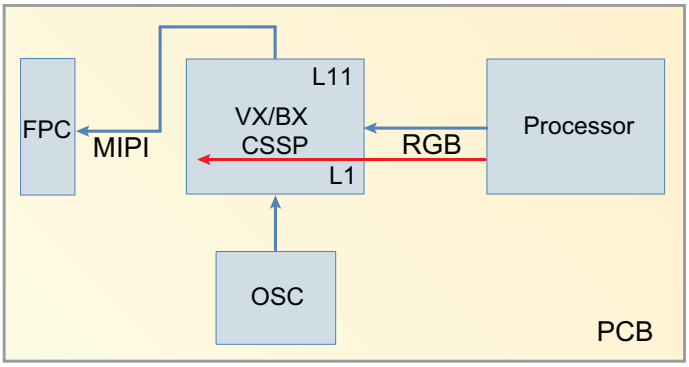


Figure 7: Poor Orientation Example



Via Technology

While advanced via technologies are more expensive that regular thru-hole via, they can be used to improve layers routing. Use blind via and/or buried via for a design that has constraints on PCB size (thus requiring routing of a signal under the ArcticLink III VX/BX CSSP). Using via-in-pad for ArcticLink III VX/BX CSSP pins that need internal layer connections.

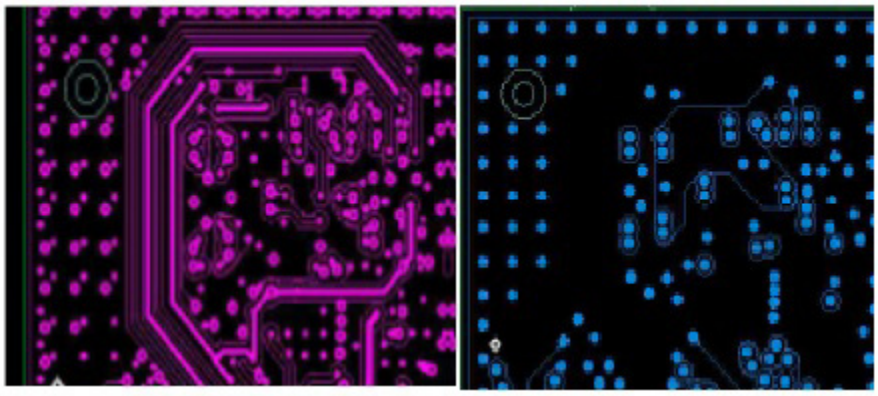
Power and Ground Planes

Dedicated power and ground planes yield the best impedance control and zero IR drop. However, these dedicated planes increases the thickness, and layers count for the PCB.

To reduce the need for a dedicated power plane, use thick traces for power routing. The thickness must meet the current requirements and be as wide as space allows.

To reduce the need for a dedicated ground plane, provide guards around the traces for each layer and fill the rest of the layer with copper (see **Figure 8**). Where possible, provide vias to tie these ground islands on each layer together. While this grounding method is not effective for EMI and trace impedance control, it provides plenty of grounding for the logics.

Figure 8: Fill-In Ground Examples



PCB Size

While increasing the board size can increase the cost of the PCB, this increase can be offset by the reduction of layers. Increasing board size provides additional routing areas and room for parts placement.

Summary

Several examples of successful implementation using the ArcticLink III VX/BX CSSPs are as follows:

- ArcticLink III VX5B3D: A four-layer board that employs a combination of good placement, blind-via, and increased PCB size to the maximum space allowed, eliminating the need for a dedicated power plane.
- ArcticLink III VX3B3B: A six-layer form-factor board that employs a combination of blind-via and buried-via, eliminating the need for a dedicated power plane.
- ArcticLink III VX3B3B: An eight-layer board that employs good placement.
- ArcticLink III VX5A2B and VX5B1D: Ten-layer boards that employ good placement.

NOTE: All of these examples employ via-in-pad.

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