QuickLogic® Programmable Fabric Power Consumption

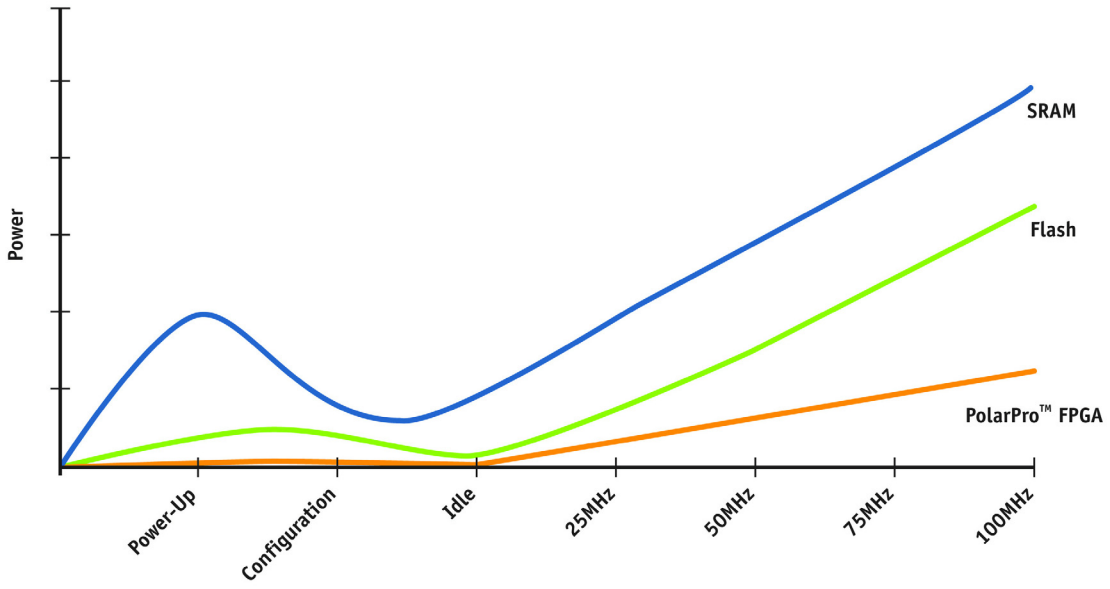
QuickLogic® White Paper

Power Demo Board Compares FPGA and CPLD Core Consumption

The need to integrate additional functionality within ever-decreasing space drives designers of portable electronics increasingly towards programmable fabric solutions. Yet devices such as FPGAs have traditionally been notoriously power-hungry, thereby restricting their use in favor of expensive-to-develop ASICs. But today, architectural and process technology advances allow a new generation of FPGAs to match or improve competing solutions, while retaining the ease-of-design, application flexibility, and low cost that accompanies programmable fabric. As a result, designers wanting to maximize their competitive advantage must balance the resources that a programmable fabric solution provides against the power that it consumes—an exercise that is far from straightforward.

Five key factors cause PLDs, and reprogrammable SRAM-based FPGAs in particular, to consume excessive amounts of power. These key factors are comprised of inrush and configuration current at device start-up along with static, dynamic, and idle mode power consumption during normal operation (see **Figure 1**).

Figure 1: FPGAs Built Using Nonvolatile Memories Consume Far Less Power than SRAM-Based Devices



Inrush current refers to the power that is consumed right after the device is powered up, and configuration current is necessary to initialize the device. Because loading device configuration data consumes appreciable power often for tens of milliseconds, reprogrammable SRAM-based FPGAs are far inferior in this respect to programmable metal-to-metal antifuse-based technologies that power up instantly. Static power refers to the current that the device consumes while there is no activity at its clock inputs and I/O pins. By comparison with antifuse technologies, the large number of registers necessary to retain device configuration data negatively affects the power consumption of reprogrammable devices, with static power measurements often running to tens or even hundreds of milliamperes.

Reprogrammable devices lose out in the dynamic power race too, since the metal-to-metal interconnections within antifuse devices offer far lower capacitances than the equivalent structures within reprogrammable device fabrics. Driving these larger parasitic capacitances account for a major portion of the system power consumption. Idle power refers to the current that a device draws when there is activity on its I/O pins, yet the device is not active. These five factors impact the overall system power budget, from battery runtimes to the external components that ensure a reliable supply of power to the device. **Table 1** shows a summary of the different power consumption states.

Table 1: Power State Consumption Summary

Power State	I/O Activity	CLK Activity
Static	No I/Os toggling	No CLKs running
Idle	I/Os toggling	No internal CLKs running
Dynamic	I/Os toggling	CLKs running

When in Doubt, Measure It

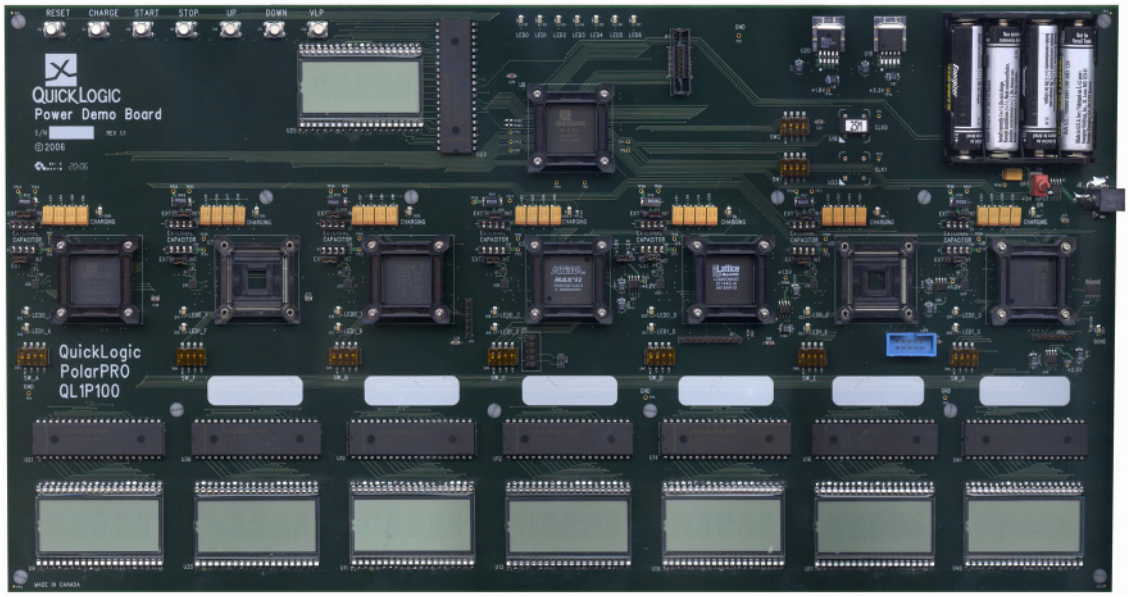
How can designers verify power consumption in today's array of device architectures? The obvious route is to take a set of evaluation boards, program their devices with functionally identical code, and measure the power drain at a common clock frequency. Unfortunately, this approach comes with practical problems. One reason is that the devices must be reasonably similar in resource and performance terms, but the availability of directly comparable evaluation boards makes this condition hard to meet. However, it is still reasonable to test each device under equivalent conditions and extrapolate, if necessary, any significant differences that may unfairly influence results. For instance, not every device has embedded SRAM, so the test code should avoid using this facility. From the hardware measurement viewpoint, only two evaluation boards (from Altera® and QuickLogic) carry current monitoring circuitry that separates the programmable device from its support components, such as dedicated voltage regulators and hardware interfaces to a host computer.

Engineers wanting to obtain accurate results when using any other evaluation board must find a way to separate the programmable device from the remainder of the board, in such a way as to allow inserting a current monitor. Package density and PCB layout issues such as common power planes can complicate or exclude this approach. While it is possible to find a common level for I/O power supplies such as 3.3 V for LVTTL compatibility, the different core voltages (1.2 V, 1.8 V, and 2.5 V) complicate assessing the power consumption of the core. Also, it is not easy to change the clock frequency on some boards.

Assessing the power consumption of crucial support circuitry such as clock-input conditioners and JTAG interfaces can be difficult, therefore many data sheets do not define this data. Xilinx and Lattice define VccAUX pins, which can consume up to 10 mA using 2.8 V or 3.3 V according to the manufacturer's data sheets. These auxiliary power supply pins power up a variety of internal circuits.

Recognizing these issues led designers at QuickLogic to produce the company's Power Demo Board, which visually compares the consumption of up to six 144-pin TQFP devices with QuickLogic's similarly packaged QL1P100 Customer Specific Standard Product (CSSP) platform (see **Figure 2**).

Figure 2: QuickLogic's Power Demo Board Provides a Visual Indication of FPGA Core Current Consumption



Devices to compare potentially include the Actel® A3P125 from their ProASIC®3 series, the Altera EPM570 from their MAX® II family, the Lattice® LCMX0640 from their MachXO™ series, and the Xilinx® XC2C384 from their CoolRunner™-II portfolio. A quick comparison between the facilities that these devices provide in their 144-pin versions is shown in **Table 2**.

Table 2: Device Comparison

Device	Logic Resources	Memory
Actel A3P125	125 K Gates	SRAM 36 K bits
Altera EPM570	570 LE	Flash 8 K bits
Lattice LCMX0640	640 LUT	SRAM 6 K bits
QuickLogic QL1P100	100 K Gates	SRAM 36 K bits
Xilinx XC2C384	384 Macrocells	None

To ensure device equality for the power measurement exercise, QuickLogic implemented test code that uses all of the lowest capacity part's 384 macrocells and then ported identical code to the other parts, thereby avoiding using any memory or other additional resources. This VHDL code comprises a standard 20-bit up counter with enable, and asynchronous and synchronous reset inputs. Since this design only uses part of even the lowest capacity device, a cyclic redundancy check (CRC) generator block fills the remainder of the available logic cells. The counter block clocks the CRC block to provide a measure of core current consumption under dynamic conditions for the core alone, thereby excluding the consumption of the various I/O blocks to yield a true picture of relative device efficiency.

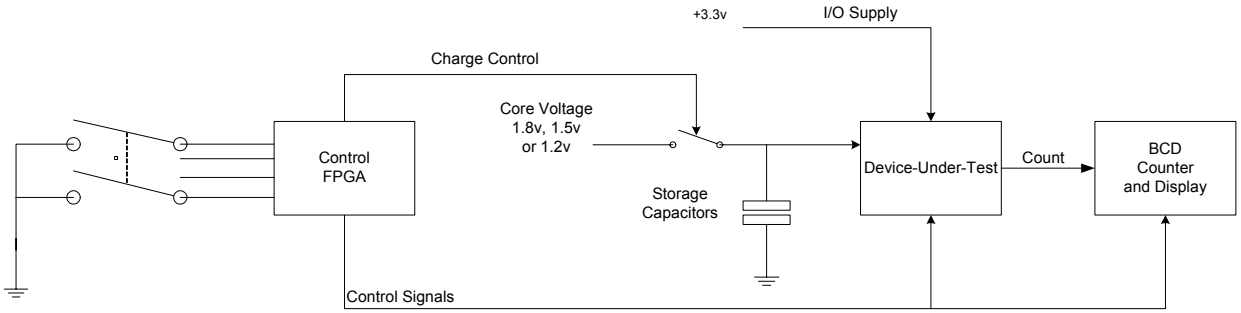
It is important to consider the different types of interconnection that the alternative device architectures implement within their fabric to ensure that, for instance, there are fair distributions of clock and control signals. This is the reason the test code uses the default routing options for each chip's development environment, rather than hand-crafting any one of them to bias results. **Appendix A —Test Code and Schematics** on page 11 contains a more detailed view of the code and its associated schematics.

Power Demo Board Hardware—Theory of Operation

A charge counter technique is employed by the QuickLogic Power Demo Board to test a device's core current consumption. The system controller is a QuickLogic QL8150 CSSP platform that implements state machine control in response to user inputs from an array of seven push button switches that simultaneously control each device-under-test (DUT) as well as the subsystems that supply power to each test socket. For each test socket, the control system charges a 4,000 mF capacitor bank to its full potential (sockets and jumpers permit users to substitute their own choice of capacitors). This stored charge supplies the device's core power supply pins with 1.2 V, 1.5 V, or 1.8 V as necessary, with the I/O and auxiliary supplies receiving 3.3 V as normal from permanent levels.

Pressing the test start button disconnects the supply to the capacitor bank and each DUT starts to count up from zero. The outputs of each DUT control and clock an ICM7224 decade counter chip that drives an LCD. Each counter increments until the charge on the capacitors feeding its core falls to a level that is incapable of sustaining operation, at which time its display freezes. The count values that accumulate represent the time taken to reach each core's drop-out point, with longer times representing lesser power consumption (see **Figure 3**).

Figure 3: A Charge Counter Provides a Visual Indication of a DUT's Power Drain



To enable users to test power consumption at different frequencies, the Power Demo Board's DIP switch SW2 applies a 4-bit code to the control FPGA that divides the master oscillator's 25 MHz reference frequency by 16, 32, 512, or 8,192. These division ratios apply nominal clock frequencies to the DUTs of 1.5625 MHz, 781.25 kHz, 48.828 kHz, and 3.052 kHz. Sockets allow users to substitute oscillator modules of their choice.

The 20-bit counter's output is tapped at the 14th stage to divide the default 1.5625 MHz input frequency by 16,384 to drive an ICM7224 binary-coded decimal (BCD) counter chip at ~95 Hz to provide a responsive display. As previously noted, this output signal also drives the CRC chain to stimulate additional power drain. The results from a series of 20 measurement runs made at 1.5625 MHz are shown in **Table 3**.

Table 3: Dynamic Mode Test Results on Low Power Board

Device[a]	Average	Max.	Min.
Altera EPM570	80	80	80
Lattice LCMX0640	62.25	65	62
QuickLogic QL1P100 CSSP Platform	412.45	415	407
Xilinx XC2C384	98.50	99	98

a. The Actel ProASIC 3 (A3P125) device results are not included due to device availability problems.

Very Low Power (VLP) Mode Slashes Static Power Drain

Because the QuickLogic PolarPro CSSP platform includes a VLP mode, the Power Demo Board includes logic that demonstrates the effectiveness of this proprietary feature. The VLP mode effectively isolates the I/O ring from the logic core, retaining the states of all the I/Os, memory and registers. This is especially useful for bus applications such as IDE or PCI controllers. While the bus operates as normal, the PolarPro CSSP platform consumes negligible power until its facilities are needed. Within 300 µsec of the VLP pin going low, the device consumes as low as 2.2 µA in standby mode while retaining the states of all logic cells, I/O registers, and memory cells. Normal operation resumes within 300 µsec of VLP going high. In this mode the PolarPro CSSP platform maintains the values of any output pad at the last known value before entering VLP mode.

A manual VLP test mode puts the PolarPro CSSP platform into its VLP state while stopping the clock to all other devices (idle mode). The user controls when to stop counting and the period between re-starting, which provides a relative indication of the respective device's leakage current when inactive. For an initial count of about 60 before stopping for ten seconds then re-starting, the typical results are shown in **Table 4**.

Table 4: Idle/VLP Mode Test Results o n Low Power Board

Device[a]	Count
Altera EPM570	60
Lattice LCMX0640	65
QuickLogic QL1P100 CSSP Platform	408
Xilinx XC2C384	89

a. The Actel ProASIC 3 (A3P125) device results are not included due to device availability problems.

Conventional Current Measurements

If these results graphically demonstrate the relative power consumption of the respective cores, it is instructive to measure their dynamic drain under equivalent conditions in a more conventional way. By removing several jumpers and substituting an external power supply, the Power Demo Board allows users to isolate and measure each core's power consumption at common clock frequencies. Note that despite data sheet claims that some of the DUTs are hot-swappable and immune to power-up sequencing issues, experience shows that repeated attempts to power up can be necessary when using an external core supply. Also, some devices draw current levels of more than twice the normal operating mode while in an indeterminate start prior to successful start-up.

In general, core current should be applied very shortly before or concurrently with I/O power. It may be necessary to try this several times and adjust the core current supply level before some devices will power up. The Power Demo Board confirms power-up by lighting the appropriate channel's LED0_x (during count operation, LED0_x and its partner LED_1x toggle at the DUT's output division frequency). The PolarPro CSSP platform does not claim power supply sequencing immunity, but appears to be the least sensitive and easiest part to start under these uncontrolled conditions. Therefore, it is prudent to monitor the supply current and be prepared to disconnect it quickly if conditions look likely to endanger the DUT. Also, monitor the voltage level into the chip, since the voltage drop across a typical 5.5-digit DMM on its 10 mA range can be significant. Given this level of resolution, consider using the 100 mA range, which typically uses a 1 Ohm sense resistor that incurs ten times less voltage burden than the 10 mA range.

While availability problems have thus far prevented testing a representative Actel part, making connections between the Power Demo Board and the available Actel's ProASIC3E development board permits a direct comparison with this board's A3PE600 device. The exercise also demonstrates the benefits that the Power Demo Board furnishes in terms of usability—for instance, to separate the A3PE600's core supply from its I/O supply requires lifting pins 8 and 9 of voltage regulator U15. These fragile pins lie on 0.65 mm pitch, and require special care to lift and re-attach them without damaging the board. Also, notice that the Actel A3PE600 requires a 1.5 V core supply and the Lattice LCMX0640 requires a 1.2 V core supply while all the other Power Demo Board devices run from 1.8 V. **Table 5** shows the core current consumption results.

Table 5: Dynamic Mode Core Current Consumption Results[a]

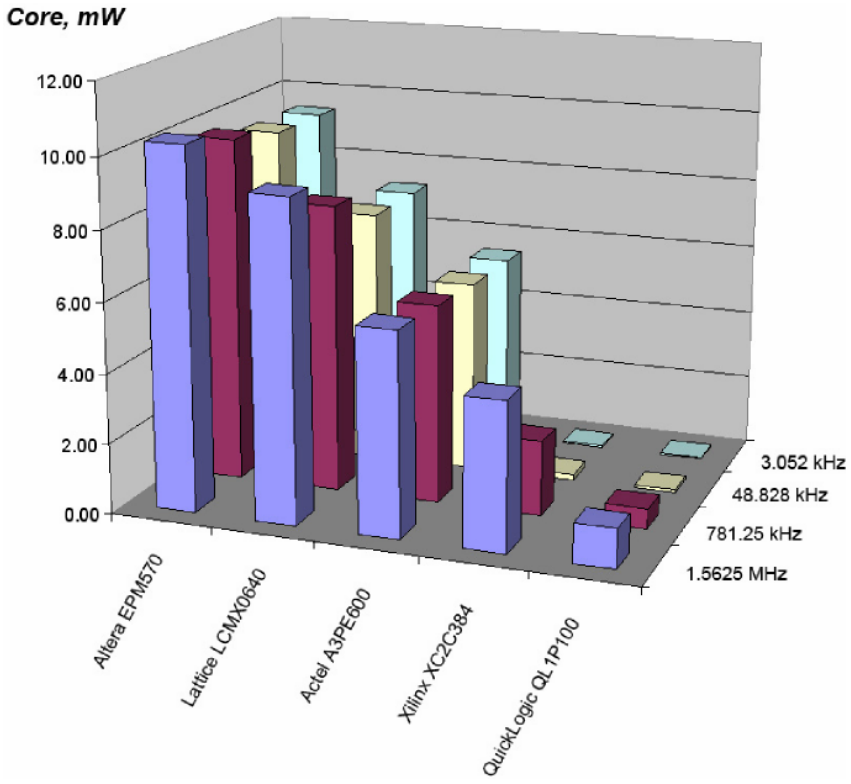
Device	1.5625 MHz	781.25 kHz	48.828 kHz	3.052 kHz
Actel A3PE600 (1.5 V)	3.8735 mA	3.7827 mA	3.6490 mA	3.6254 mA
Altera EPM570 (1.8 V)	5.7176 mA	5.4661 mA	5.2501 mA	5.2389 mA
Lattice LCMX0640 (1.2 V)	7.6101 mA	6.8235 mA	6.0540 mA	6.0485 mA
QuickLogic QL1P100 CSSP Platform (1.8 V)	0.6215 mA	0.3216 mA	0.0417 mA	0.0242 mA
Xilinx XC2C384 (1.8 V)	2.3558 mA	1.1833 mA	0.0918 mA	0.0254 mA

a. Current measurements are for the core VCC supply only, and do not include any auxiliary or I/O power supplies.

What is the Secret?

Several factors combine to make the PolarPro CSSP platform more power efficient than other chips. The most obvious of these is the use of QuickLogic's proprietary ViaLink technology, a six-layer metal-to-metal interconnection system. Since there is no need for memory to retain the device's configuration, this reduces static power consumption. It also greatly reduces dynamic power consumption, because the metal-to-metal interconnection possesses very low capacitance when compared with arrays of transistor cells. This advantage is easy to see in **Figure 4**, which charts the respective devices' core current consumption in mW versus the test frequency.

Figure 4: Core Power Consumption in mW at Four Test Frequencies[1]



1. Power measurements are for the core VCC supply only, and do not include any auxiliary or I/O power supplies.

More exhaustive tests at QuickLogic's laboratory extend these measurements up to 100 MHz as shown in **Table 6**.

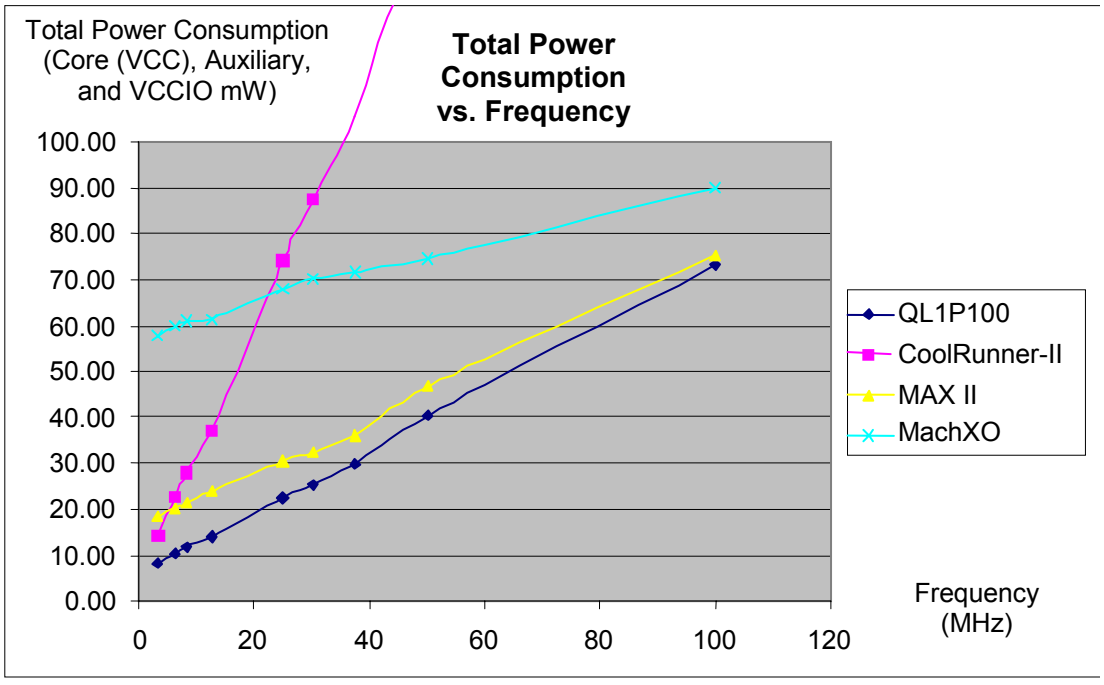
Table 6: Power Drain (Core mW) at Different Frequencies[a]

Device[b]	3.12 MHz	6.25 MHz	8.25 MHz	12.5 MHz	25 MHz	30 MHz	37.5 MHz	50 MHz	100 MHz
QuickLogic QL1P100 CSSP Platform	7.93	10.12	11.72	14.02	22.41	25.25	29.80	40.60	73.03
Xilinx XC2C384 (1.8 V)	14.45	22.62	28.01	36.96	74.39	87.53	105.61	146.69	254.50
Altera EPM570 (1.8 V)	18.52	20.18	21.34	23.79	30.67	32.34	35.95	46.87	75.49
Lattice LCMX0640 (1.2 V)	57.74	59.80	61.20	61.37	67.84	70.40	71.79	74.72	90.06

a. Power measurements include all the power supply (VCC, auxiliary, and VCCIO) needed for a particular device.
b. The Actel ProASIC 3 (A3P125) device results are not included due to device availability problems.

As shown in **Figure 5**, graphically expressing these results highlights the frequency-dependent natures of the current drain that the respective devices exhibit.

Figure 5: Total FPGA Power Drain Strongly Depends on Clock Frequency



Remember that static and dynamic power consumption are just two of the major factors that determine the overall system power budget. Other factors include inrush current, configuration power, and static/idle mode consumption. Because its antifuse settings configure PolarPro CSSP platforms, there is no need for the power-up configuration phase that SRAM-based devices require, which dispenses with inrush and configuration currents. Also, most consumer applications need to put the device into a power-saving mode during its operation. PolarPro CSSP platforms include a unique VLP mode that cuts power consumption to microamp levels while retaining all state information.

Furthermore, devices such as the QL1P200 CSSP platform and larger add a SafeGate™ clock gating circuit that allows designers to dynamically enable and disable each clock signal within the device. This arrangement allows active logic within the device to turn on/off clock signals that supply other parts of the device, intelligently enabling significant power savings in logic segments that do not need to be active. Turning off the clocks when they are not needed at the input pad saves the power that is dissipated in clock-routing resources as well as in any logic blocks that the clock signals drive. In fact, most of the core's power is dissipated in driving the CSSP platform's internal clock trees. As the clock-buffer enable signals are available internally, there is no need for external logic to implement this control.

Most importantly, PolarPro CSSP platforms include deglitching circuitry to allow the clocks to be turned on and off asynchronously, without fear of false edges triggering unstable or unwanted conditions. Without this feature, clock gating techniques typically require extensive planning and partitioning between logic modules. This feature is transparent to the user. As a result, designers can easily deploy PolarPro CSSP platforms in low power systems and maximize their power saving advantages by applying simple on/off controls to control active and sleep mode states.

PolarPro CSSP Platform Key Features

The PolarPro CSSP platform family currently comprises six devices with densities from 512 to 7,680 logic cells, which is equivalent to 75,000 to 1 million gates. The PolarPro CSSP platform family offers from 8 to 22 RAM modules with a similar number of FIFO controllers to support from 36,684 to 202,752 bits of dual-port RAM. Users can concatenate RAM resources vertically and horizontally to build memories of arbitrary width and depth, with independently configurable read and write clocks and selectable pipelined or non-pipelined read data. Each PolarPro CSSP platform furnishes two user-configurable clock managers for the multiple low-skew clock networks that employ global and quadrant-based routing. Four programmable global clock networks complement a single dedicated global clock network, with each quadrant similarly having one dedicated and four programmable clock networks for a maximum of 20 quad clock networks per device. Package options range from a 132-pin TFPGA that supports up to 77 user I/Os to a 324-pin LBGA for as many as 238 user I/Os. User I/O is bank-programmable for drive current and slew rate, and supports common logic interface levels including DDR memories. Several security links are available to disconnect the on-chip JTAG system, making it virtually impossible to reverse-engineer the device's contents.

Table 7: PolarPro CSSP Platform Family Members

Features		QL1P075	QL1P100	QL1P200	QL1P300	QL1P600	QL1P1000
Max Gates		75,000	100,000	200,000	300,000	600,000	1,000,000
Logic Cells		512	640	1,536	1,920	4,224	7,680
Max I/O		172	188	292	302	508	652
RAM Modules		8	8	12	12	24	24
FIFO Controllers		8	8	12	12	24	24
RAM bits		36,864	36,864	55,296	55,296	221,184	221,184
CCMs		2[a]	2[a]	2	2	2	2
Packages	TFBGA (0.5 mm)	132	132	132	132	-	-
	TQFP (0.5 mm)	144	144	-	-	-	-
	TFBGA (0.8 mm)	196	196	-	-	-	-
	LBGA (1.0 mm)	256	256	256, 324	256, 324	256, 324	256, 324

a. The PolarPro 144-pin TQFP and 132-pin TFBGA devices have one CCM. The PolarPro 196-pin TFBGA, 256-pin LBGA and 324-pin LBGA devices have two CCMs.

Table 8: PolarPro CSSP Platform Family Maximum Usable I/Os

Device	132 TFBGA (8 mm x 8 mm)	144 TQFP	296 TFBGA (12 mm x 12 mm)	256 LBGA	324 LBGA
QL1P075	77	97	136	168	-
QL1P100	77	97	136	184	-
QL1P200	74	-	-	184	238[a]
QL1P300	74	-	-	184	238[a]
QL1P600	-	-	-	184[a]	238[a]
QL1P1000	-	-	-	184[a]	238[a]

a. Preliminary

Table 9: PolarPro CSSP Platform Family Packaging Options

Device Information	Device					
	QL1P075/QL1P100		QL1P200/QL1P300		QL1P600/QL1P1000	
	Pin	Pitch	Pin	Pitch	Pin	Pitch
Package Definitions[a]	132 TFBGA (8 mm x8 mm)	0.50 mm	132 TFBGA (8 mm x8 mm)	0.50 mm	256 LBGA	1.0 mm
	144 TQFP	0.50 mm	256 LBGA	1.0 mm	324 LBGA	1.0 mm
	196 TFBGA (12 mm x 12 mm)	0.80 mm				
	256 LBGA	1.0 mm				

a. TFBGA = Thin Profile Fine Pitch Ball Grid Array
LBGA = Low Profile Ball Grid Array
TQFP = Thin Quad Flat Pack

Appendix A —Test Code and Schematics

Each DUT on the Power Demo Board uses identical VHDL code. This code consists of two main blocks:

- A 20-bit up counter, with reset and enable—the output of this block clocks the input clock of an external ICM7224 BCD counter.
- A 21-stage cyclic-redundancy-check (CRC) unit.

External pins supply each 20-bit counter's input clock and reset signals, while the counter's output clocks the CRC units as well as the external BCD counter chip.

The logic for the CRC block consists of this VHDL code:

```
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_unsigned.all;

entity crc16 is port (
   rst:     in std_logic;
   clk:     in std_logic;
   gen_en:  in std_logic;
   out en:  in std_logic;
   din:     in std_logic;
   dout:    out std_logic; );
end crc16;

architecture rtl of crc16 is

signal crc_reg : std_logic_vector(15 downto 0);

begin

   dout <= crc_reg(15);

process(rst, clk)
   begin
        if(rst = '1') then
             crc_reg <= (others=>'0');
   elsif rising_edge(clk) then
   -- generates the CRC
        if(gen_en ='1') then
             crc_reg(15 downto 13) <= crc_reg(14 downto 12);
             crc_reg(12)<= din xor crc_reg(15) xor crc_reg(11);
             crc_reg(11 downto 6) <= crc_reg(10 downto 5);
             crc_reg(5)<= din xor crc_reg(15) xor crc_reg(4);
             crc_reg(4 downto 1) <= crc_reg(3 downto 0);
             crc_reg(0)<= din xor crc_reg(15);
   -- shifts the CRC out
        elsif(out_en = '1') then
             crc_reg(15 downto 1) <= crc_reg(14 downto 0);
             crc_reg(0)<='0';
```

```
        end if;
    end if;
end process;
end rtl;
```

The counter is a standard 20-bit up counter with enable, and asynchronous and synchronous resets:

```
COUNT_PROCESS: process(rst,clk)
begin
    if (rst='1') then
        i_cnt(others=>'0');
    elsif rising_edge(clk) then
        if(standby_mode_on = '0') then
            if (i_start_re='1') then
                i_cnt<= (others=>'0');
            elsif (start='1') then
                i_cnt <= i_cnt + '1';
            end if;
        end if;
    end if;
end process;
```

The remainder of the code generates resets etc.

Figure 6: crc16.vhd Schematic

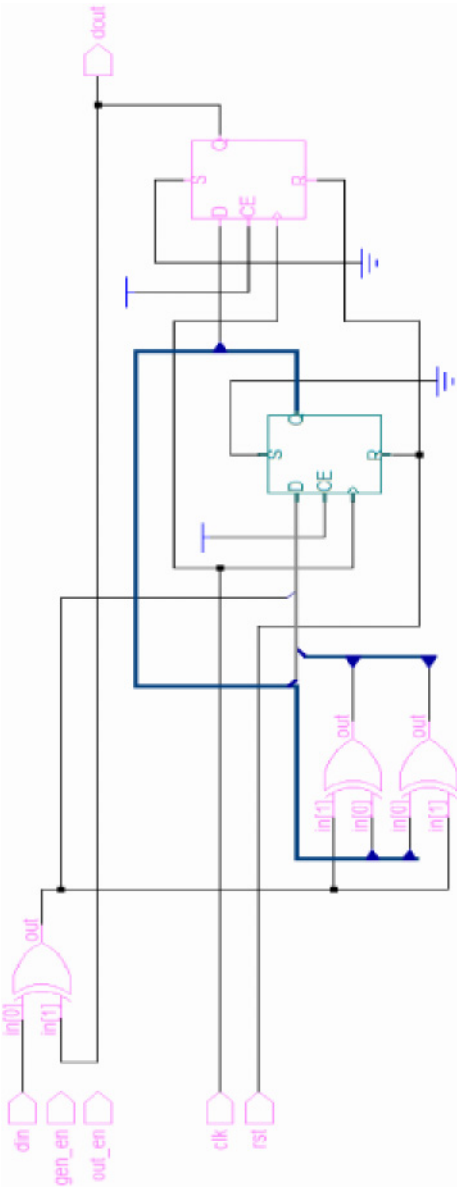


Figure 7: Full Schematic (1 of 3)

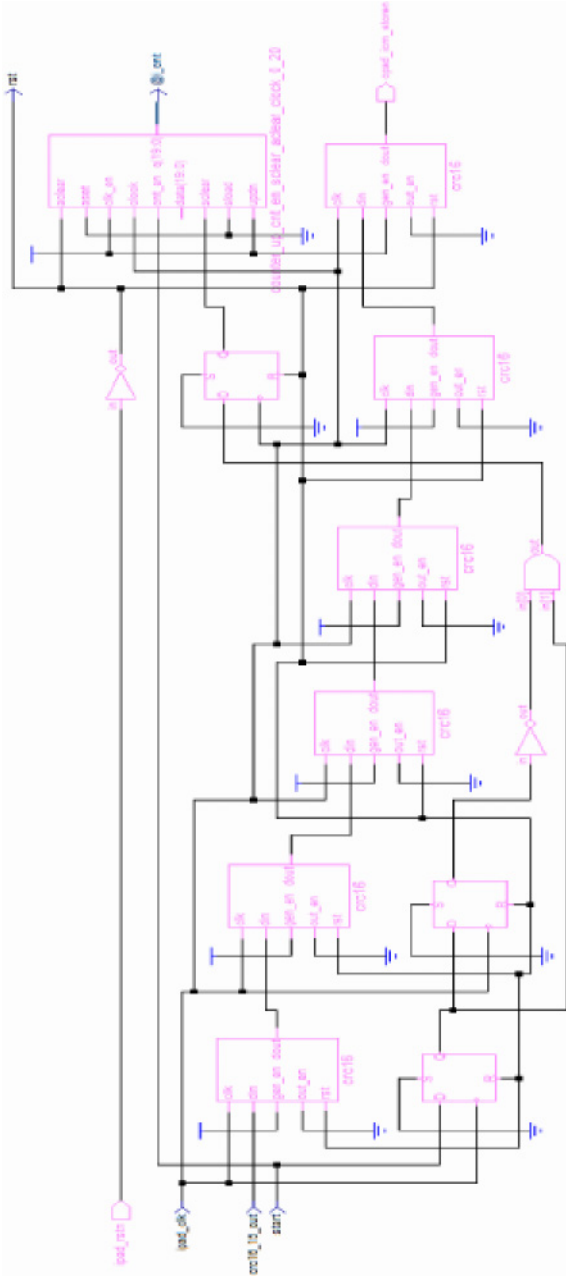


Figure 8: Full Schematic (2 of 3)

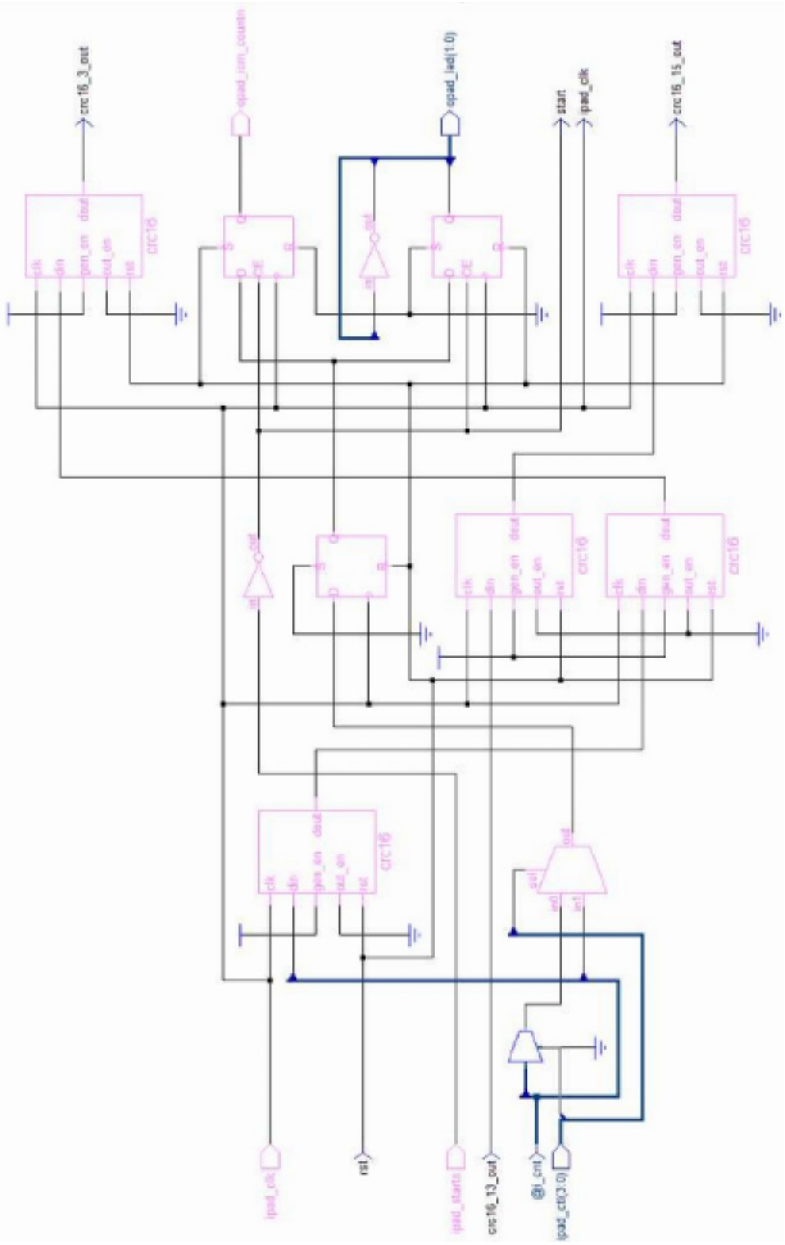
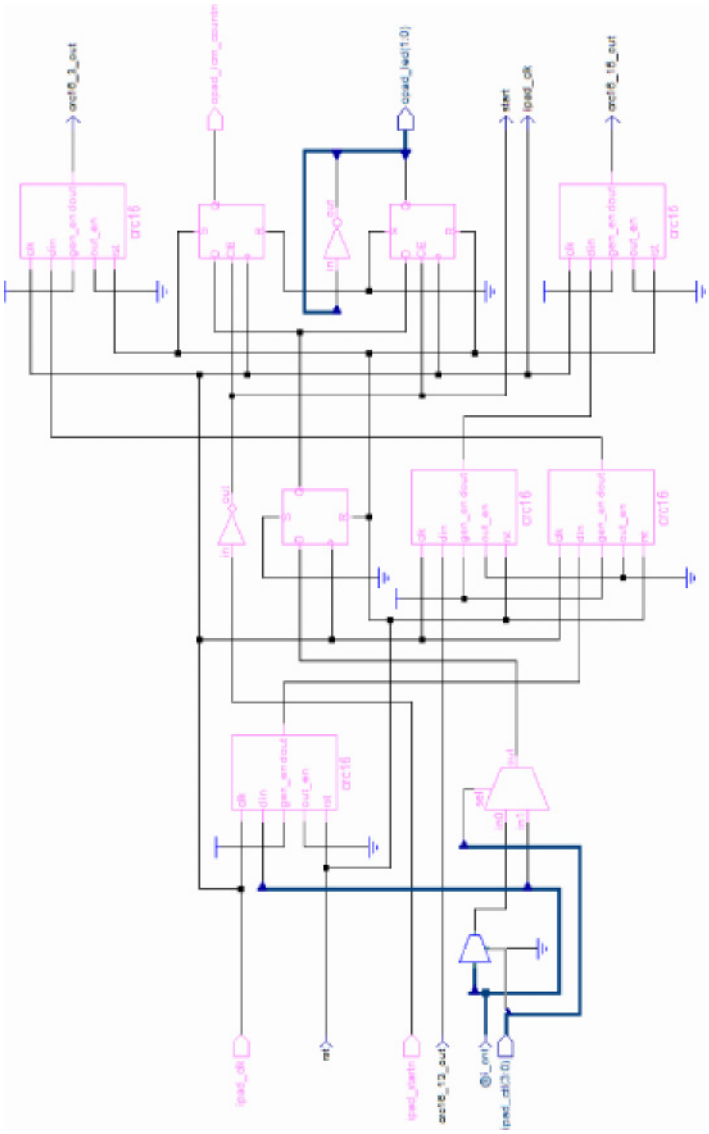


Figure 9: Full Schematic (3 of 3)



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Revision History

Revision	Date	Originator and Comments
A	February 2007	Robert Dawson and Kathleen Murchek
B	January 2009	Kathleen Murchek Updated banner, contact info, trademark info and added notice of disclaimer.

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