PolarPro® Solution Platform Family Data Sheet

Family of Solution Platforms Integrating Low Power Programmable Fabric and Embedded SRAM

Platform Highlights

Flexible Programmable Fabric

- 8 to 240 customizable building blocks (CBBs) (see **Programmable Fabric Architectural Overview** on page 5 for a detailed explanation of CBBs)
- As low as 2.2 µA standby current
- 1.8 V core voltage, 1.8/2.5/3.3 V drive capable I/Os
- 9 Kbits to 220 Kbits of SRAM
- Embedded synchronous/asynchronous FIFO controllers
- Up to two user configurable clock managers (CCMs) (see **Configurable Clock Manager** on page 6 for an explanation of CCM)
- 48 to 244 programmable I/Os available
- Ideal platform to implement additional proven system blocks (PSBs), custom functions, glue logic and processor interface

Programmable I/O

- Bank programmable drive strength
- Bank programmable slew rate control
- Independent I/O banks capable of supporting multiple I/O standards in one platform
- Native support for DDRIOs in some packages
- Bank programmable I/O standards: LVTTL, LVCMOS, LVCMOS18, PCI, SSTL2, SSTL3 and SSDL18
- Can be used for level shifter and I/O voltage translator

Very Low Power (VLP) Mode

- The QuickLogic PolarPro Solution Platform family has a special VLP pin which can enable a low power sleep mode that significantly reduces the overall power consumption of the platform by placing the platform in standby.
- Enter/exit VLP mode from/to normal operation in less than 250 µs (typical).

JTAG

QuickLogic PolarPro Solution Platform family supports IEEE 1149.1 boundary scan or post-manufacturing testability. External access to this feature can be completely disabled.

Solution Highlights

- Integrated, single-chip solution for multiple peripheral host controllers and interfaces to reduce both system BOM cost and board space.
- Programmable fabric for proven system blocks and custom functions.
- Fast time-to-market with QuickLogic's complete low power connectivity solutions.

Solution Platform Combining Programmable Fabric, Embedded SRAM and Advanced Clock Management

The PolarPro family of solution platforms meets the interconnect, host control and power management requirements of power sensitive and portable applications. The PolarPro Solution Platform family offers a spectrum of platforms with varying amounts CBBs for implementing PSBs, custom functions and glue logic. QuickLogic provides a portfolio of PSBs such as PCI, IDE, NAND controller, high-speed SPI and Bluetooth2.X UART.

QuickLogic's lowest power programmable fabric, based on QuickLogic's patented ViaLink™ technology, provides ultimate flexibility, allowing customers to quickly make changes to their system and differentiate their products from their competitors.

Table 1 summarizes the PolarPro Solution Platform family features.

Table 1: PolarPro Solution Platform Family

Platform	QL8050	QL1P100	QL1P300	QL1P1000
Customizable Building Blocks	8	20	60	240
Max I/Os	124	188	302	652
RAM Bits	9,216	36,864	55,296	221,184
CCMs	0	2	2	2
Packages	100 VQFP (14x14 mm) 101 CTBGA (6x6 mm) 144 TQFP (20x20 mm) 196 TFBGA (12x12 mm)	121 TFBGA (6x6 mm) 132 TFBGA (8x8 mm) 144 TQFP (20x20 mm) 196 TFBGA (12x12 mm) 256 LBGA (17x17 mm)	99 WLCSP 132 TFBGA (8x8 mm) 256 LBGA (17x17 mm)	324 LBGA (19x19 mm)

Table 2 shows the maximum usable I/Os available in each package.

Table 2: Maximum Usable I/Os

Platform	99 WLCSP	100 VQFP	101 CTBGA	121 TFBGA	132 TFBGA	144 TQFP	196 TFBGA	256 LBGA	324 LBGA
QL8050	-	62	72	-	-	100	124	-	-
QL1P100	-	-	-	76	77	97	136	184	-
QL1P300	63			-	74	-	-	184	-
QL1P1000	-	-	-	-	-	-	-	-	244

Table 3 summarizes the type of proven system blocks for each technology segment provided by QuickLogic.

Table 3: Proven System Blocks Provided by QuickLogic

Proven System Blocks for Each Technology Segment	
Storage	**Intelligence**
• IDE/P-ATA Host Controller	• Direct Memory Access (DMA)
• CE-ATA Host Controller	• Smart Data Transfer (SDT)
• NAND Flash Controller	• Data Aggregator (DA)
• Secure Digital (SD) Card Host Controller	**Security and Custom Options**
• Compact Flash (CF) Host Controller	• Content Protection for Recordable Media (CPRM)
• Multimedia Card (MMC) Controller	• Serial ID
• Memory Stick (MS) Controller	**Network**
• Managed NAND Controller with Boot Capability	• SDIO Client
• Optical Drive Controller (ATAPI)	• High-Speed SDIO Controller
Video and Imaging	• MiniPCI for Ethernet, Wi-Fi/WiMAX Controller
• Visual Enhancement Engine (VEE)	• SPI Controller
• X/Y Swap	• Bluetooth 2.x + EDR High-Speed UART
• High-Definition LCD Controller	

The QuickLogic PolarPro Solution Platforms offer a wide range of fabric capacities as shown in **Figure 1**.

Figure 1: QuickLogic PolarPro Solution Platforms

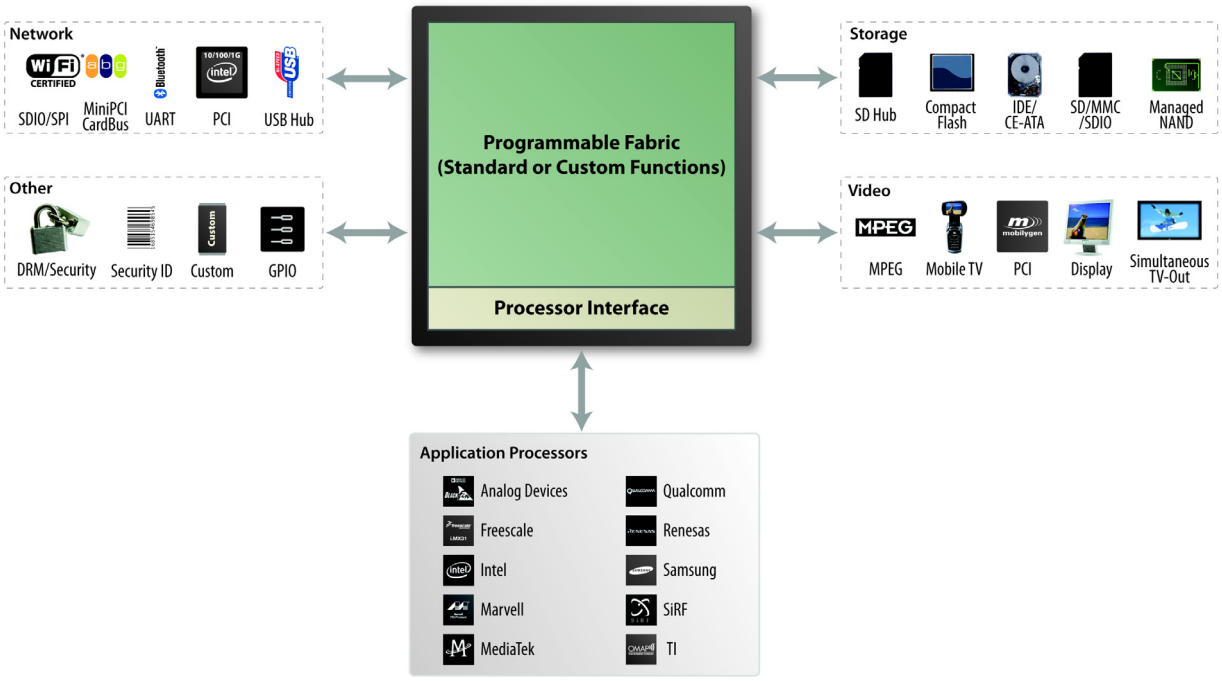
Applications Overview

QuickLogic's PolarPro family of programmable solution platforms were specifically architected with flexibility in mind. The platforms work seamlessly with any processor available in the market today, and contain a programmable fabric that allows designers to address any emerging connectivity requirement. These versatile platforms enable connectivity solutions for IDE, SD/SDIO/MMC, High Speed UART, SD/SDIO/MMC Hub, PCI, CE-ATA, NAND Flash, Compact Flash and MPEG interfaces while still offering a small form factor package and low power technology. These platforms are suitable for portable/mobile consumer and industrial electronics applications (see **Figure 2**).

This highly flexible architecture makes it the ideal platform to implement processor companion solutions for smartphones, portable media players (PMP), portable navigation devices (PND), controllers, ePOS terminals, wireless data cards and ExpressCards.

The PolarPro Solution Platform family can be used to replace several discrete components, reducing BOM cost and saving board space. It gives developers the ability to harness a wide variety of interfaces with ultra-low power consumption. QuickLogic also provides proven system blocks, software drivers, documentation, reference schematics and support to help accelerate time-to-market.

Figure 2: PolarPro Connectivity Solutions



Full System Design Support

QuickLogic provides a full range of services and libraries to address a development team's needs such as hardware design support, software drivers, and packaging.

On the hardware development front, QuickLogic supports customers in two ways. First, its Customer Solutions Architects (CSAs) help development teams determine the best way to utilize a CSSP platform in their design. Working closely with the development team's designers, the CSAs help create detailed specifications for the functionality and performance of a customized CSSP.

Once the specifications are complete, QuickLogic's System Solution Team (SST) steps in to implement the design. The SST handles the details of configuring the personality of hard-logic blocks, implementing additional standard functions in the programmable fabric, and implementing the customer's unique functions in the fabric. Support from the SST carries through the design phase into test and system integration. SST members work along side customer development team members at the customer site to ensure that the customized CSSP functions as intended.

To aid a development team's software development effort, QuickLogic supports its CSSPs and library logic blocks with a full range of device drivers. Drawing on its experience with Windows® CE, Windows Mobile®, and Linux® operating systems, QuickLogic has created drivers for each OS for every block. The drivers are optimized for the CSSP implementation and are fully supported during the customer's hardware/software integration phase.

Programmable Fabric Architectural Overview

The QuickLogic PolarPro Solution Platform family features a high performance and low power programmable fabric to implement additional proven system blocks. The programmable fabric consists of a range from 8 to 240 customizable building blocks (CBB) to implement combinations of different interfaces required by the customer design specifications, which results in a much higher integration, more flexibility and lower system BOM costs. A CBB is a unit of measurement that represents the on-chip logic that can be used to implement a variety of proven system blocks (such as SDIO, PCI, IDE, CE-ATA and NAND Flash controller), custom logic, or other system level functions (see **Table 3** on page 3 for a list of proven system blocks).

RAM Modules

The PolarPro Solution Platform family has 4-Kbit (4,608 bits) RAM blocks which are used primarily as buffers and FIFOs to significantly improve system performance. The RAM features include:

- Independently configurable read and write data bus widths
- Independent read and write clocks
- Horizontal and vertical concatenation
- Write byte enables
- Selectable pipelined or non-pipelined read data
- Ability to generate true dual-port RAMs through concatenation with completely independent read/write ports and clock domains

Embedded FIFO Controllers

Every RAM block can be implemented as a synchronous or asynchronous FIFO. There are built-in FIFO controllers that allow for varying depths and widths without requiring programmable fabric resources.

The PolarPro Solution Platform family FIFO controller features include:

- x9, x18 and x36 data bus widths
- Independent PUSH and POP clocks
- Independent programmable data width on PUSH and POP sides
- Configurable synchronous or asynchronous FIFO operation
- 4-bit PUSH and POP level indicators to provide FIFO status outputs for each port
- Pipelined read data to improve timing

Configurable Clock Manager

The CCM includes a Phase Locked Loop (PLL) component, a frequency multiplier, and phase modifier. The PLL is a closed loop frequency control system that detects the phase difference between the input and output signals and aligns them. The frequency multiplier adds the ability to multiply the input frequency by a configurable factor of two or four. Additionally, the phase modifier supports the ability to shift the output frequency phase and offset by a given time delay.

The CCM features include:

- Input frequency range from 25 MHz to 200 MHz
- Output frequency range from 25 MHz to 200 MHz
- Output jitter is less than 200 ps peak-to-peak
- Two outputs: pullout0 (with 0° phase shift), and pullout1 (with an option of 0°, 90°, 180°, or 270° phase shift plus a programmable delay).
- Programmable delay allows delays up to 2.5 ns at 250 ps intervals
- Output frequency lock time in less than 10 µs

The reset signal can be routed from a clock pad or generated using internal logic. The lock_out signal can be routed to internal logic and/or an output pad. CCM clock outputs can drive the global clock networks, as well as any general purpose I/O pin. Once the CCM has synchronized the output clock to the incoming clock, the lock_out signal will be asserted to indicate that the output clock is valid. Lock detection requires at least 10 µs after reset to assert lock_out. The PolarPro Solution Platform family CCM has three modes of operation, based on the input frequency and desired output frequency. **Table 4** indicates the features of each mode.

Table 4: CCM PLL Mode Frequencies

Output Frequency	Input Frequency Range	Output Frequency Range	PLL Mode
x1	25 MHz to 200 MHz	25 MHz to 200 MHz	PLL_MULT1
x2	15 MHz to 100 MHz	30 MHz to 200 MHz	PLL_MULT2
x4	10 MHz to 50 MHz	40 MHz to 200 MHz	PLL_MULT4

Very Low Power (VLP) Mode

The QuickLogic PolarPro Solution Platform family has a unique feature, referred to as VLP mode, which reduces power consumption by placing the platform in standby. Specifically, VLP mode can bring the programmable fabric standby current down to less than 2.2 µA at room temperature when no incoming signals are toggled. VLP mode is controlled by the VLP pin. The VLP pin is active low, so VLP mode is activated by pulling the VLP pin to ground. Conversely, the VLP pin must be pulled to 3.3 V for normal operation.

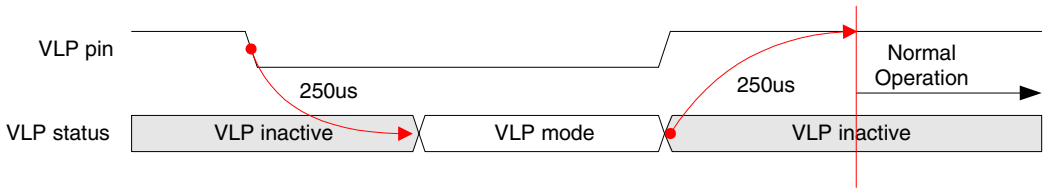
When the PolarPro Solution Platform family goes into VLP mode, the following occurs:

- All register values in the programmable fabric and GPIO are preserved
- All RAM cell data is retained
- The outputs from all GPIO to the internal logic are tied to a weak '1'
- GPIO outputs drive the previous values
- GPIO output enables retain the previous values
- Clock pad inputs are gated
- The CCM is held in the reset state

The entire operation from normal mode to VLP mode requires 250 µs (300 µs maximum). As mentioned in the VLP behavioral description above, the output of the GPIO to the internal logic is a weak '1'. Therefore, to preserve data retention GPIO should not be used for a set, reset, or clock signal.

As the Solution Platform exits out of VLP mode, the data from the registers, RAM, and GPIO will be used to recover the functionality of the platform. Furthermore, since the CCM is in a reset state during VLP mode, it will have to re-acquire the correct output signals before asserting lock_out. The time required to go from VLP mode to normal operation is 250 µs (300 µs maximum). **Figure 3** displays the delays associated with entering and exiting VLP mode.

Figure 3: Typical VLP Mode Timing



Electrical Specifications

DC Characteristics

The DC Specifications are provided in **Table 5** through **Table 10**.

Table 5: Absolute Maximum Ratings

Parameter	Value	Parameter	Value
VCC Voltage	-0.5 V to 2.2 V	Latch-up Immunity	±100 mA
VCCIO Voltage	-0.5 V to 4.0 V	ESD Pad Protection	2 kV
VREF Voltage	-0.5 V to 2.0 V	Leaded Package Storage Temperature	-65° C to + 150° C
Input Voltage	-0.5 V to 4.0 V	Laminate Package (BGA) Storage Temperature	-55° C to + 125° C

Table 6: Recommended Operating Range

Symbol	Parameter	Military		Industrial		Commercial		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
VCC	Supply Voltage	1.71	1.89	1.71	1.89	1.71	1.89	V
VCCIO	I/O Input Tolerance Voltage	1.71	3.60	1.71	3.60	1.71	3.60	V
TJ	Junction Temperature	-55	125	-40	100	0	85	°C

Table 7: Recommended Power Supply Ripple Noise

Symbol	Parameter	Conditions	Min.	Max.	Unit
VCC	Digital Supply Voltage	ALL	-50	+50	mV
CCMVCC	Analog Supply Voltage for the Fabric	<4 MHz	-10	+10	mV
		>4 MHz	-30	+30	mV
		<160 MHz	-30	+30	mV

Table 8: QL8050 DC Characteristics

Symbol	Parameter	Conditions	Min	Max	Units
I_I	I or I/O Input Leakage Current	VI = VCCIO or GND	-1	1	µA
I_{OZ}	3-State Output Leakage Current	VI = VCCIO or GND	-	1	µA
C_I	I/O Input Capacitance	-	-	8	pF
C_{CLOCK}	Clock Input Capacitance	-	-	8	pF
I_{OS}	Output Short Circuit Current[a]	VO = GND VO = VCC	-15 40	-180 210	mA mA
I_{REF}	Quiescent Current on INREF	-	-10	10	µA
I_{PD}	Current on programmable pull-down	VCC = 1.8 V	-	50	µA
I_{PUMP}	Quiescent Current on VPUMP	VPUMP= 3.3 V	-	10	µA
I_{VCCIO}	Quiescent Current on VCCIO	VCCIO = 3.3 V VCCIO = 2.5 V VCCIO = 1.8 V	-	20 10 10	µA

a. The data provided in **Table 8** represents the JEDEC and PCI specifications. Duration should not exceed 30 seconds.

Table 9: QL1P100, QL1P300, and QL1P1000 DC Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
I_I	I or I/O Input Leakage Current	VI = VCCIO or GND	-	-	1	µA
I_{OZ}	3-State Output Leakage Current	VI = VCCIO or GND	-	-	1	µA
C_I	I/O Input Capacitance	VCCIO = 3.6 V	-	-	10	pF
C_{CLOCK}	Clock Input Capacitance	VCCIO = 3.6 V	-	-	10	pF
I_{REF}	Quiescent Current on INREF	-	-	-	5	µA
I_{PD}	Current on programmable pull-down	VCCIO = 3.6 V	-200	-	-50	µA
		VCCIO = 2.75 V	-150	-	-25	µA
		VCCIO = 1.89 V	-100	-	-10	µA
I_{PU}	Current on programmable pull-up	VCCIO = 3.6 V	50	-	200	µA
		VCCIO = 2.75 V	25	-	150	µA
		VCCIO = 1.89 V	10	-	100	µA
I_{VLP}	Quiescent Current on VLP pin	VLP=3.3	-	1	10	µA
I_{CCM}	Quiescent Current on each CCMVCC	VCC=1.89 V	-	1	10	µA
I_{VCC}	Quiescent Current for QL1P100	VLP=GND	-	2.2	40	µA
		VLP=3.3V	-	40	100	µA
	Quiescent Current for QL1P300	VLP=GND	-	TBD	TBD	µA
		VLP=3.3V	-	TBD	TBD	µA
	Quiescent Current for QL1P1000	VLP=GND	-	25	-	µA
		VLP=3.3V	-	200	-	µA
I_{VCCIO}	Quiescent Current on VCCIO	VCCIO = 3.6 V	-	2	10	µA
		VCCIO = 2.75 V	-	2	10	µA
		VCCIO = 1.89 V	-	2	10	µA

Table 10: DC Input and Output Levels[a]

Symbol	INREF		V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V_{MIN}	V_{MAX}	V_{MIN}	V_{MAX}	V_{MIN}	V_{MAX}	V_{MAX}	V_{MIN}	mA	mA
LVTTL	n/a	n/a	-0.3	0.8	2.2	VCCIO + 0.3	0.4	2.4	2.0	-2.0
LVCMOS2	n/a	n/a	-0.3	0.7	1.7	VCCIO + 0.3	0.7	1.7	2.0	-2.0
LVCMOS18	n/a	n/a	-0.3	0.63	1.2	VCCIO + 0.3	0.7	1.7	2.0	-2.0
GTL+	0.88	1.12	-0.3	INREF - 0.2	INREF + 0.2	VCCIO + 0.3	0.6	n/a	40	n/a
PCI	n/a	n/a	-0.3	0.3 x VCCIO	0.6 x V_{CCIO}	VCCIO + 0.5	0.1 x VCCIO	0.9 x VCCIO	1.5	-0.5
SSTL2	1.15	1.35	-0.3	INREF - 0.18	INREF + 0.18	VCCIO + 0.3	0.74	1.76	7.6	-7.6
SSTL3	1.3	1.7	-0.3	INREF - 0.2	INREF + 0.2	VCCIO + 0.3	1.10	1.90	8	-8

a. The data provided in **Table 10** represents the JEDEC and PCI specification. QuickLogic platforms either meet or exceed these requirements.

Figure 4 shows the quiescent current of the QL8050 for each of the voltage supplies, across voltage and temperature. Quiescent current on V_{CC} is a function of platform utilization. The numbers in the following graph was taken from 100% utilized platforms, filled with 32-bit counters. For conditions other than those described, measured quiescent current levels may be higher than the values in **Figure 4**.

Figure 4: Quiescent Current on V_{CC} for QL8050

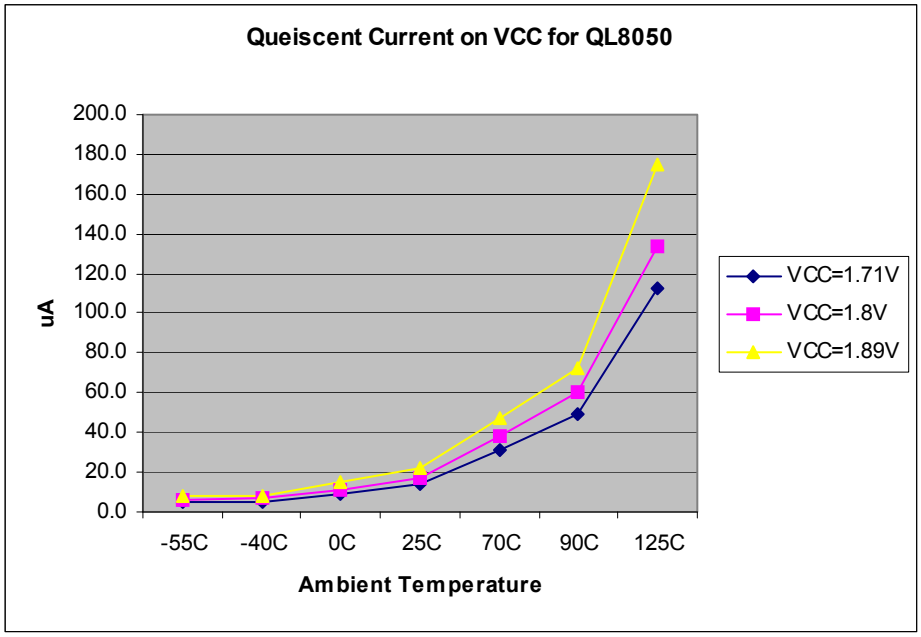


Table 11: Quiescent Current on V_{CC} for QL8050 (Over All Temperatures – Over 1.71 V to 3.6 V)

Parameter	Current
IVDED	2.6 µA
ICCIO	2.0 µA

Figure 5 and **Figure 6** illustrate quiescent current for QL1P100 with VLP = 0 V and 3.3 V.

Figure 5: Quiescent Current for QL1P100 with VLP = 0 V

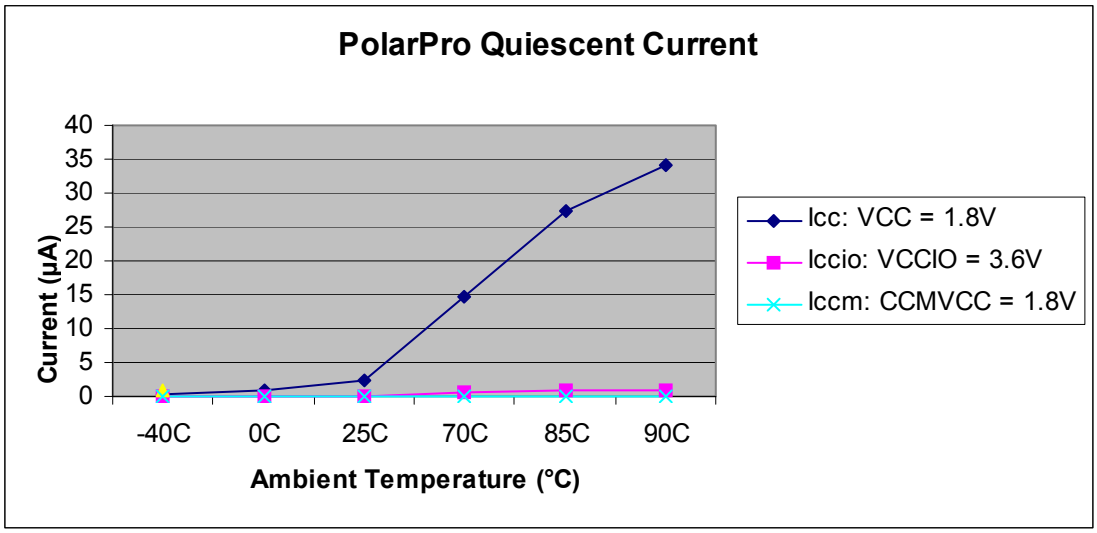


Figure 6: Quiescent Current for QL1P100 with VLP = 3.3 V

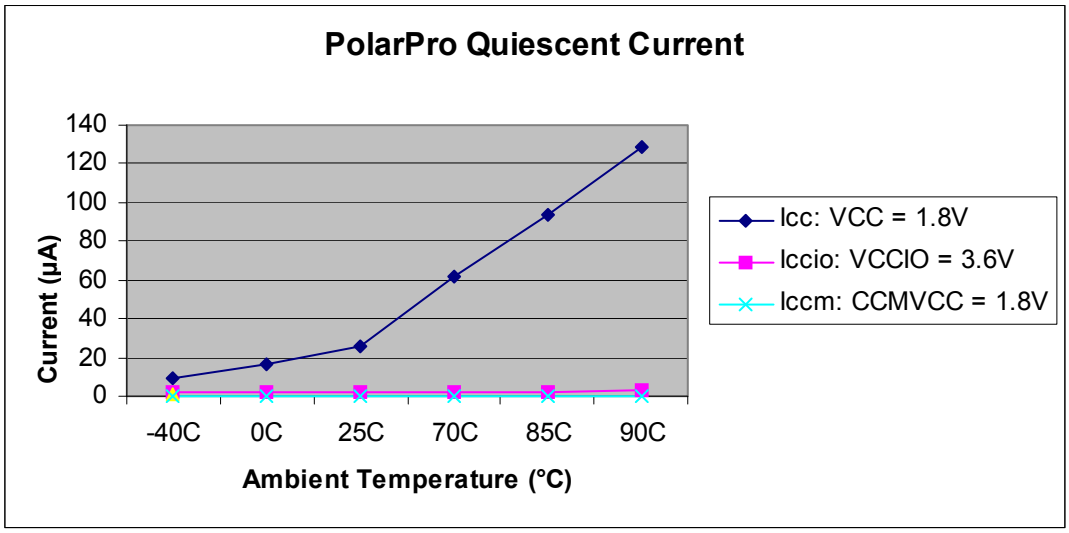


Figure 7 and **Figure 8** illustrate quiescent current for QL1P300 with VLP = 0 V and 3.3 V.

Figure 7: Quiescent Current for QL1P300 with VLP = 0 V

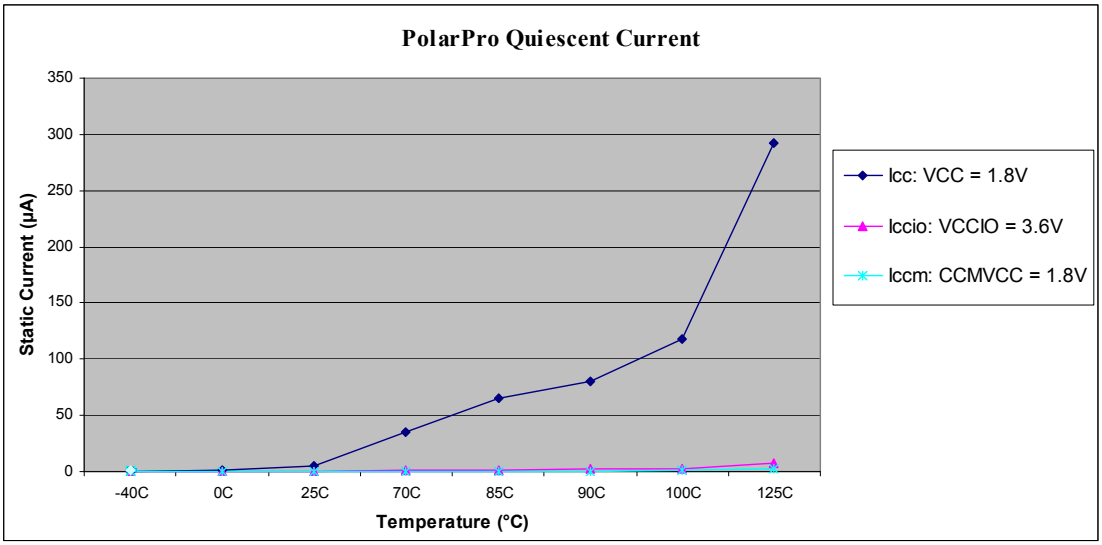
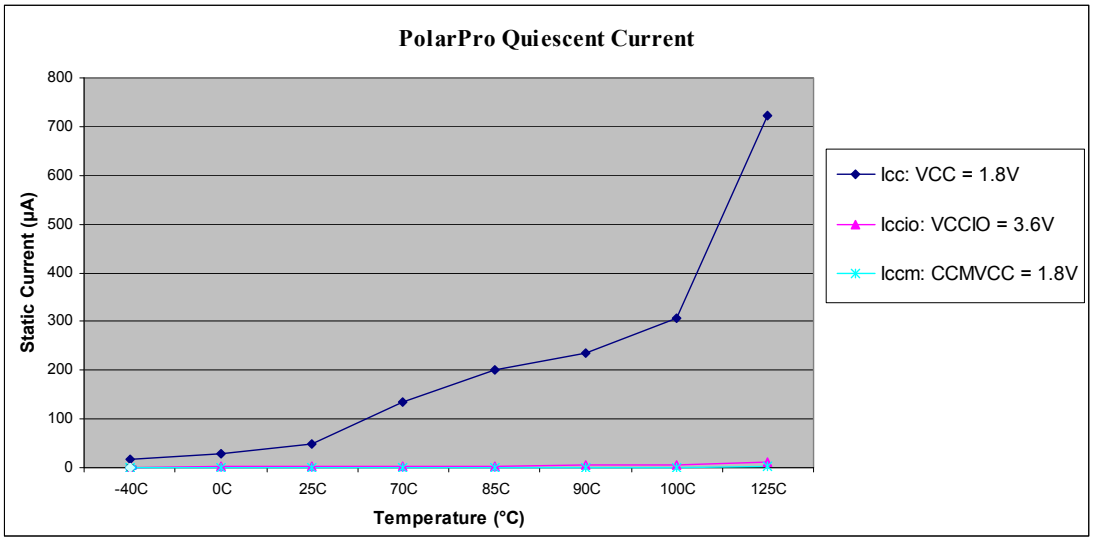


Figure 8: Quiescent Current for QL1P300 with VLP = 3.3 V



AC Characteristics

Clock Tree Timing

Table 12 shows the Fabric PLL timing requirements.

Table 12: Fabric PLL Timing Requirements

Symbol	Parameter	Min.	Max.	Unit
$t_{JITTER\_FB\_CLK}$	100 MHz FB_CLK jitter tolerance	-	150	ps

Package Thermal Characteristics

The PolarPro Solution Platform family is available for Commercial (0°C to 85°C Junction) and Industrial (-40°C to 100°C Junction) temperature ranges.

Thermal Resistance Equations:

$\theta_{JA} = (TJ - TA)/P$

$P_{MAX} = (T_{JMAX} - T_{AMAX})/\theta_{JA}$

Parameter Description:

θ_{JA}: Junction-to-ambient thermal resistance

T_J: Junction temperature

T_A: Ambient temperature

P: Power dissipated by the platform while operating

P_{MAX}: The maximum power dissipation for the platform

T_{JMAX}: Maximum junction temperature

T_{AMAX}: Maximum ambient temperature

NOTE: Maximum junction temperature (T_{JMAX}) is 100°C. To calculate the maximum power dissipation for a platform package look up θ_{JA} from **Table 13**, pick an appropriate T_{AMAX} and use: $P_{MAX} = (125°C - T_{AMAX})/ \theta_{JA}$

Table 13: Package Thermal Characteristics

Package Description				θ_{JA} (° C/W)		
Platform	Package Code	Package Type	Pin Count	0 LFM	200 LFM	400 LFM
QL8050	PT	TFBGA	196	54	51.8	48
	PF	TQFP	144	41	39	37
	PU	CTBGA	101	59	52	50
	PV	VQFP	100	43	41.3	38.8
QL1P100	PU	TFBGA	121	54	47	45
	PU	TFBGA	132	55	48	46
	PF	TQFP	144	50	44	42
	PT	TFBGA	196	42.0	35.0	33.5
	PS	LBGA	256	48.2	41.7	40.2
QL1P300	WU	WLCSP	99	31	27	25
	PU	TFBGA	132	44	37	35
	PS	LBGA	256	35.5	29.0	27.7
QL1P1000	PS	LBGA	324	24	18	17

Power Consumption

Programmable Fabric Power Consumption

QuickLogic's ultra low power programmable fabric is ideal for implementing connectivity solutions, custom logic and processor interface. The standby current of the smallest PolarPro Solution Platform fabric in VLP mode is as low as 2.2 µA. The dynamic power consumption varies depending on the operating conditions and what functions are used in the fabric.

Power-Up Sequencing

Figure 9: Power-Up Sequencing

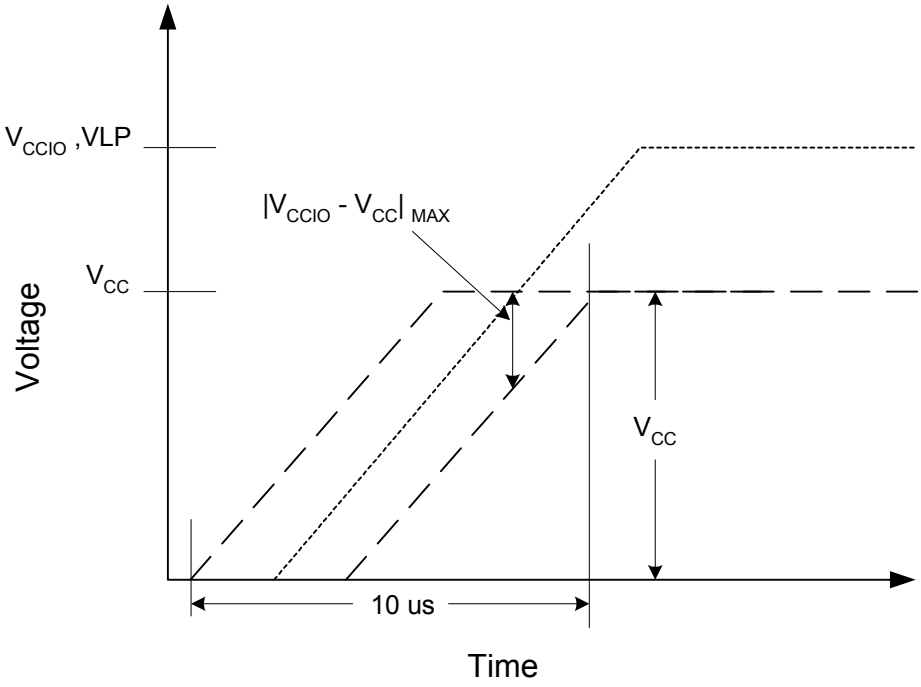


Figure 9 shows an example where all VCCIO = 3.3 V.

When powering up the PolarPro Solution Platform, VCC, VCCIO rails must take 10 µs or longer to reach the maximum value (refer to **Figure 9**). Ramping VCC and VCCIO faster than 10 µs can cause the platform to behave improperly.

It is also important to ensure VCCIO and VLP are within 500 mV of VCC when ramping up the power supplies. In the case where VCCIO or VLP are greater than VCC by more than 500 mV an additional current draw can occur as VCC passes its threshold voltage. In a case where VCC is greater than VCCIO by more than 500 mV the protection diodes between the power supplies become forward biased. If this occurs then there will be an additional current load on the power supply. Having the diodes on can cause a reliability problem, since it can wear out the diodes and subsequently damage the internal transistors.

Pin Descriptions

QL8050 Pin Descriptions

Table 14 shows the various pins of the PolarPro Solution Platforms.

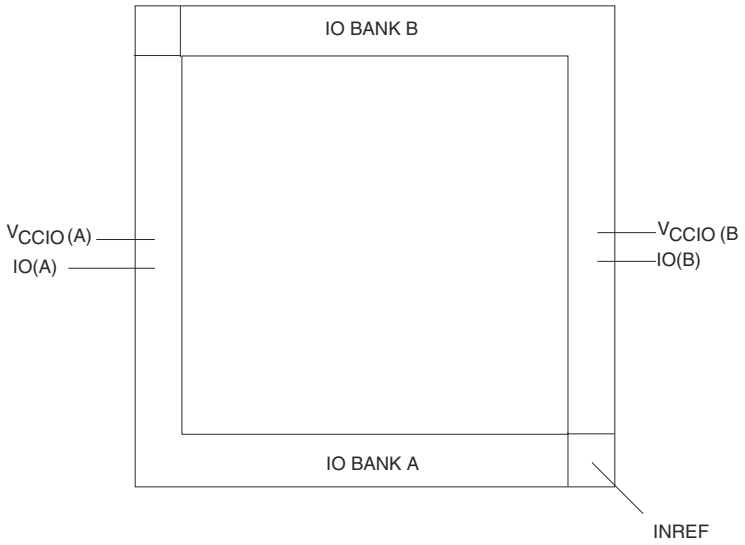
Table 14: QL8050 Pin Descriptions

Pin	Direction	Function	Description
JTAG Pin Descriptions			
TDI/RSI	I	Test Data In for JTAG/RAM init. Serial Data In	Hold HIGH during normal operation. Connects to serial PROM data in for RAM initialization. Connect to VDED2 if unused
TRSTB/RRO	I/0	Active low Reset for JTAG/RAM init. reset out	Hold LOW during normal operation. Connects to serial PROM reset for RAM initialization. Connect to GND if unused
TMS	I	Test Mode Select for JTAG	Hold HIGH during normal operation. Connect to VDED2 if not used for JTAG
TCK	I	Test Clock for JTAG	Hold HIGH or LOW during normal operation. Connect to VDED2 or GND if not used for JTAG
TDO/RCO	O	Test data out for JTAG/RAM init. clock out	Connect to serial PROM clock for RAM initialization. Must be left unconnected if not used for JTAG or RAM initialization. The output voltage drive is specified by VDED.
Dedicated Pin Descriptions			
CLK	I	Global clock network pin	Low skew global clock. This pin provides access to a dedicated, distributed network capable of driving the CLOCK, SET, RESET, F1, and A2 inputs to the Logic Cell, READ, and WRITE CLOCKS, Read and Write Enables of the Embedded RAM Blocks, and Output Enables of the I/Os. The voltage tolerance of this pin is specified by VDED. The voltage tolerance of the CLK pins in the PU101 package are specified by VCCIO(B).
I/O(A)	I/O	Input/Output pin	The I/O pin is a bi-directional pin, configurable to either an input-only, output-only, or bi-directional pin. The A inside the parenthesis means that the I/O is located in Bank A. If an I/O is not used, SpDE (Quick*Works* Tool) provides the option of tying that pin to GND, VCC, or TriState.
VCC	I	Power supply pin	Connect to 1.8 V supply.
VCCIO(A)	I	Input voltage tolerance pin	This pin provides the flexibility to interface the platform with either a 3.3 V, 2.5 V, or 1.8 V platform. The A inside the parenthesis means that VCCIO is located in BANK A. Every I/O pin in Bank A will be tolerant of VCCIO input signals and will drive VCCIO level output signals. This pin must be connected to either 3.3 V, 2.5 V, or 1.8 V.
GND	I	Ground pin	Connect to ground.
INREF(A)	I	Differential reference voltage	The INREF is the reference voltage pin for GTL+, SSTL2, and STTL3 standards. Follow the recommendations provided in **Table 10** for the appropriate standard. The A inside the parenthesis means that INREF is located in BANK A. This pin should be tied to GND if voltage referenced standards are not used.

Table 14: QL8050 Pin Descriptions *(Continued)*

Pin	Direction	Function	Description
IOCTRL(A)	I	Highdrive input	This pin provides fast RESET, SET, CLOCK, and ENABLE access to the I/O cell flip-flops, providing fast clock-to-out and fast I/O response times. This pin can also double as a high-drive pin to the internal logic cells. The A inside the parenthesis means that IOCTRL is located in Bank A. There is an internal pull-down resistor to GND on this pin. This pin should be tied to GND if it is not used. If tied to VDED, it will draw no more than 20 µA per IOCTRL pin due to current through the pull-down resistor. The voltage tolerance of this pin is specified by VDED. Note that the 208 PQFP package has no I/O control pins.
VPUMP	I	Charge Pump Disable	This pin disables the internal charge pump for lower static power consumption. To disable the charge pump, connect VPUMP to 3.3 V. If the Disable Charge Pump feature is not used, connect VPUMP to GND.
VDED	I	Voltage tolerance for clocks, TDO JTAG output, and IOCTRL	This pin specifies the input voltage tolerance for CLK, DEDCLK, and IOCTRL dedicated input pins, as well as the output voltage drive TDO JTAG pins. The legal range for VDED is between 1.71 V and 3.6 V.
VDED2	I	Voltage tolerance for JTAG pins (TDI, TMS, TCK, and TRSTB)	These pins specify the input voltage tolerance for the JTAG input pins. The legal range for VDED2 is between 1.71 V and 3.6 V. These do not specify output voltage of the JTAG output, TDO. Refer to the VDED pin section for specifying the JTAG output voltage.

Figure 10: QL8050 I/O Banks with Relevant Pins



Recommended Unused Pin Terminations for the QL8050 Solution Platform

All unused, general purpose I/O pins can be tied to VCC, GND, or HIZ (high impedance) internally using the Configuration Editor. This option is given in the bottom-right corner of the placement window. To use the Placement Editor, choose **Constraint > Fix Placement** in the **Option** pull-down menu of SpDE.

The rest of the pins should be terminated at the board level in the manner presented in **Table 15**.

Table 15: QL8050 Recommended Unused Pin Terminations

Signal Name	Recommended Termination
IOCTRL<y>[a]	There is an internal pull-down resistor to GND on this pin. This pin should be tied to GND if it is not used. If tied to VDED, it will draw no more than 20 µA per IOCTRL pin due to current through the pull-down resistor.
CLK	Any unused clock pins should be connected to VDED or GND.
INREF<y>	If an I/O bank does not require the use of the INREF signal the pin should be connected to GND.

a. y represents an alphabetical character.

QL1P100, QL1P300, and QL1P1000 Pin Descriptions

Table 16: QL1P100, QL1P300, and QL1P1000 Pin Descriptions

Pin	Direction	Function	Description
Dedicated Pin Descriptions			
GPIO(C:A)	I/O	CSSP dependent	CSSP dependent proven system block I/O.
CLK(C:A)	I	Global clock network pin low skew global clock	This pin provides access to a distributed network capable of driving the CLOCK, SET, RESET, all inputs to the Logic Cell, READ and WRITE CLOCKS, Read and Write Enables of the Embedded RAM Blocks, and I/O inputs. The voltage tolerance of this pin is specified by VCCIO(C:A).
DEDCLK(D)	I	Dedicated clock network pin low skew clock	This pin provides access to a distributed network capable of driving the CLOCK, SET, RESET, all inputs to the Logic Cell, READ and WRITE CLOCKS, Read and Write Enables of the Embedded RAM Blocks, and I/O inputs. The voltage tolerance of this pin is specified by VCCIO(D).
CCMIN(1:0)	I	CCM clock input	Input clock for CCM. The voltage tolerance for this pin is specified by the VCCIO of the same bank.
CCMVCC (1:0)	I	Power supply pin for CCM	CCM input voltage level. Configurable as 1.8 V only.
CCMGND(1:0)	I	Ground pin for CCM	Connect to ground.
VLP	I	Voltage low power	Active low. Therefore, when VLP pin is low, the platform will go into low power mode. Tie VLP to 3.3 V to disable low power mode.
VCC	I	Power supply pin	Connect to 1.8 V supply.
VCCIO(D:A)	I	Input voltage tolerance pin	This pin provides the flexibility to interface the platform with either a 3.3 V, 2.5 V, or 1.8 V platform. The letter inside the parenthesis means that the VCCIO is located in the bank with that letter. Every I/O pin in the same bank will be tolerant of the same VCCIO input signals and will drive VCCIO level output signals. This pin must be connected to either 3.3 V, 2.5 V, or 1.8 V.
GND	I	Ground pin	Connect to ground.
DQ[a]/ GPIO(D)	I/O	Configurable pin can be declared as either a DDRIO DQ or as a general purpose I/O	The D inside the parenthesis means that the I/O is located in Bank D. If an I/O is not used, the development software provides the option of tying that pin to GND, VCCIO, or Hi-Z.
DQS[a]/ GPIO(D)	I/O	Configurable pin can be declared as either a DDRIO DQS or as a general purpose I/O	The D inside the parenthesis means that the I/O is located in Bank D. If an I/O is not used, the development software provides the option of tying that pin to GND, VCCIO, or Hi-Z.
DQCK_N[a]/ GPIO(D)	I/O	Configurable pin can be declared as either a DDRIO DQ, DDR negative clock, or as a general purpose I/O.	The D inside the parenthesis means that the I/O is located in Bank D. If an I/O is not used, the development software provides the option of tying that pin to GND, VCCIO, or Hi-Z.
DQCK_P[a]/ GPIO(D)	I/O	Configurable pin can be declared as either a DDRIO DQ, DDR positive clock, or as a general purpose I/O.	The D inside the parenthesis means that the I/O is located in Bank D. If an I/O is not used, the development software provides the option of typing that pin to GND, VCCIO, or Hi-Z.

Table 16: QL1P100, QL1P300, and QL1P1000 Pin Descriptions *(Continued)*

Pin	Direction	Function	Description
VREF(D)	I	Differential reference voltage	The INREF is the reference voltage pin for the SSTL1.8 and SSTL2 standards. The D inside the parenthesis means that INREF is located in Bank D. Tie this pin to GND if voltage referenced standards are not used.
JTAG Pin Descriptions			
TDI/RSI	I	Test data in for JTAG/RAM init. serial data in	Hold HIGH during normal operation. Connect to VCCIO(B) if unused.
TRSTB	I	Active low reset for JTAG	Hold LOW during normal operation. Connect to GND if unused. During JTAG, a high voltage is based on VCCIO(B).
TMS	I	Test mode select for JTAG	Hold HIGH during normal operation. Connect to VCCIO(B) if not used for JTAG.
TCK	I	Test clock for JTAG	Hold HIGH or LOW during normal operation. Connect to VCCIO(B) or GND if not used for JTAG.
TDO	O	Test data out for JTAG	Must be left unconnected if not used for JTAG. The output voltage drive is specified by VCCIO(B).

a. The number following the DDRIO signal names in the pinout tables indicates the DDRIO set the pin corresponds to.

Recommended Unused Pin Terminations for QL1P100, QL1P300, and QL1P1000 Solution Platforms

All unused, general purpose I/O pins can be tied to VCCIO, GND, or Hi-Z (high impedance) internally. By default, QuickLogic QuickWorks software ties unused I/Os to GND.

Terminate the rest of the pins at the board level as recommended in **Table 17**.

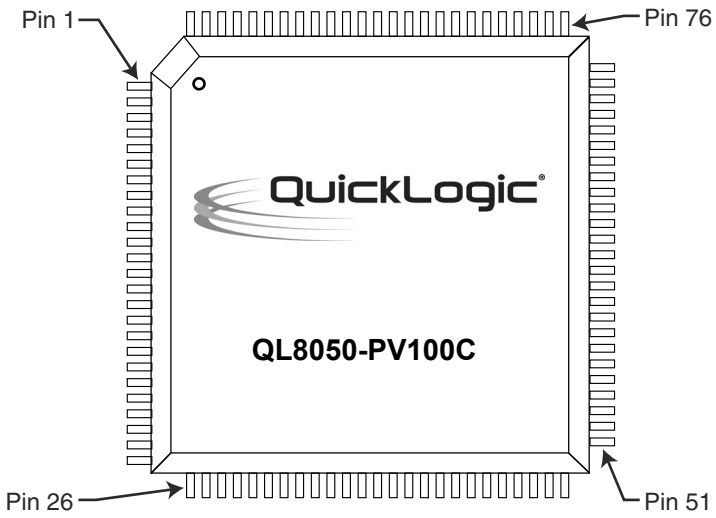
Table 17: QL1P100, QL1P300, and QL1P1000 Recommended Unused Pin Terminations

Signal Name	Recommended Termination
VREF	If an I/O bank does not require the use of the INREF signal, connect the pin to GND.
CLK <x>[a]	Connect to GND or VCCIO(x) if unused.
VLP	Tie VLP to 3.3 V to disable low power mode.
CCMVCC(1:0)	If a CCM is not used, the corresponding CCMVCC may be tied to GND to reduce power consumption. If a CCM is used, do not try to disable the CCM by tying the CCMVCC to GND.
TDI	Connect to VCCIO(B) if not used for JTAG.
TRSTB	Connect to GND if not used for JTAG.
TMS	Connect to VCCIO(B) if not used for JTAG
TCK	Connect to VCCIO(B) or GND if not used for JTAG.
TDO	Must be left unconnected if not used for JTAG.

a. x represents A, B, C or D.

Packaging Pinout Diagrams

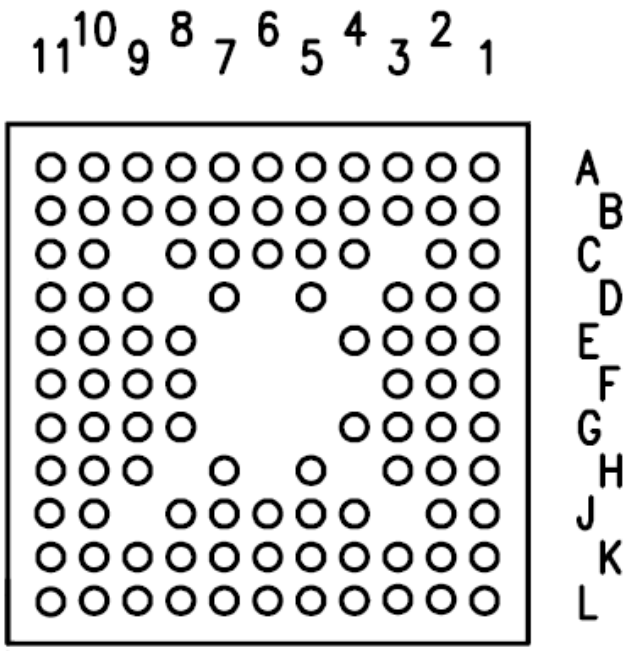
QL8050 - 100 VQFP Pinout Diagram



QL8050 - 101 CTBGA Pinout Diagram

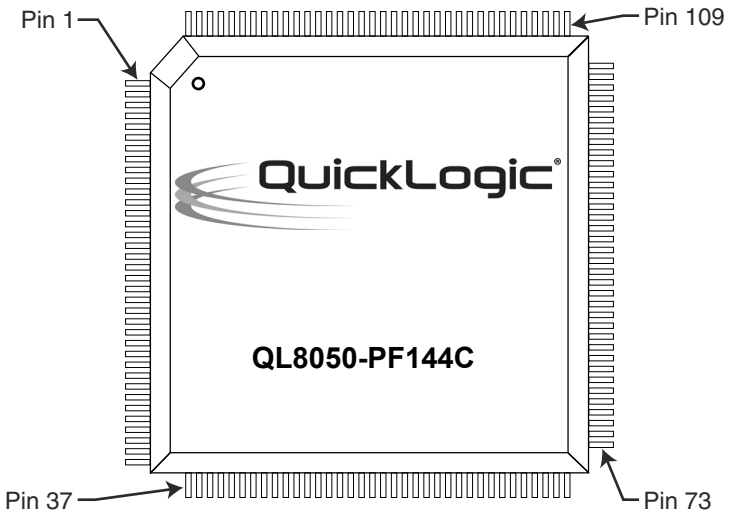
Top

Bottom



QL8050 - 144 TQFP Pinout Diagram

Top



QL8050 - 196 TFBGA Pinout Diagram

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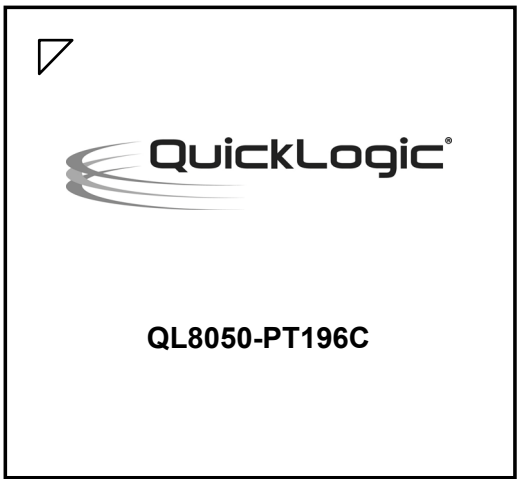

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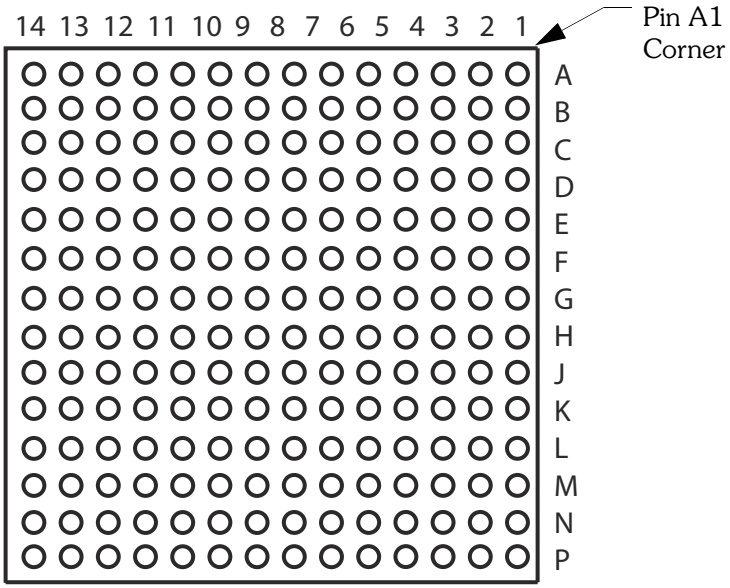
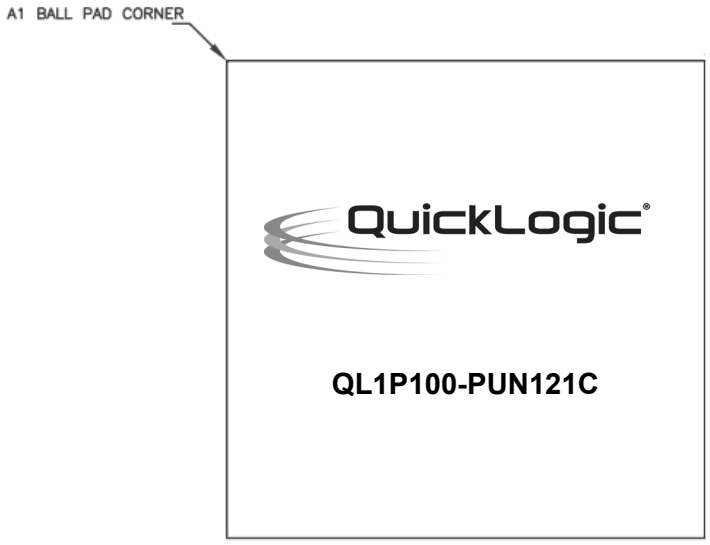


QL1P100 - 121 TFBGA Pinout Diagram

Top



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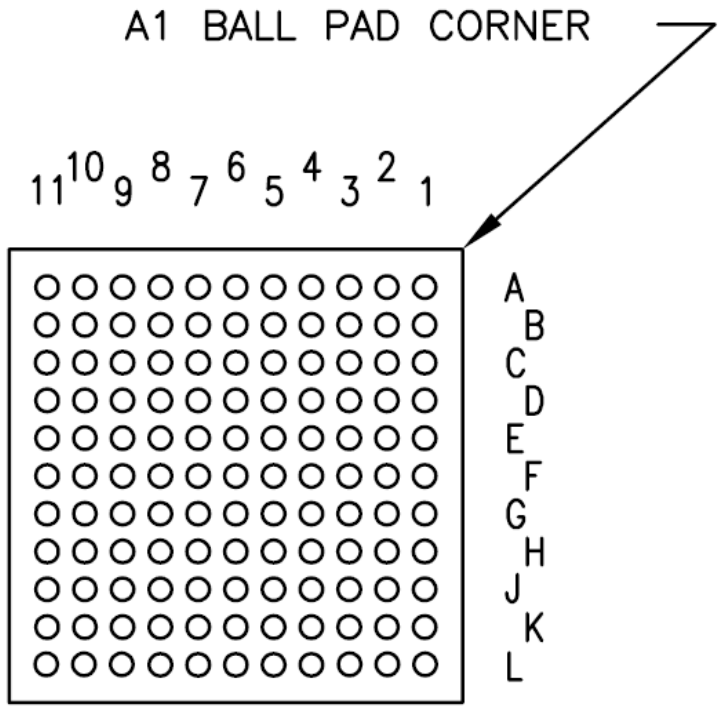
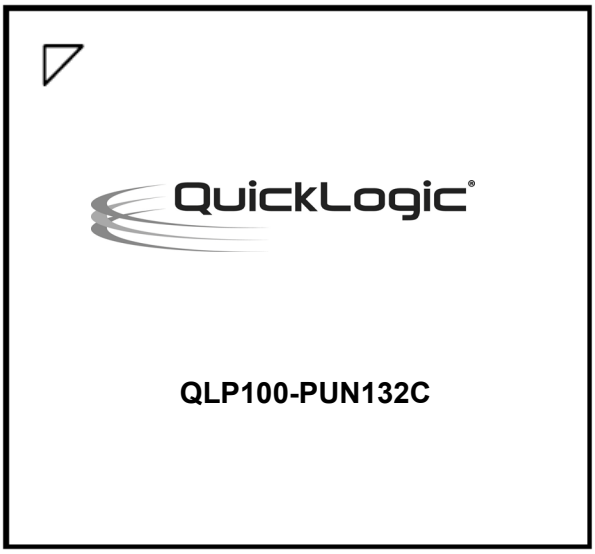


QL1P100 and QL1P300 - 132 TFBGA Pinout Diagram

Top



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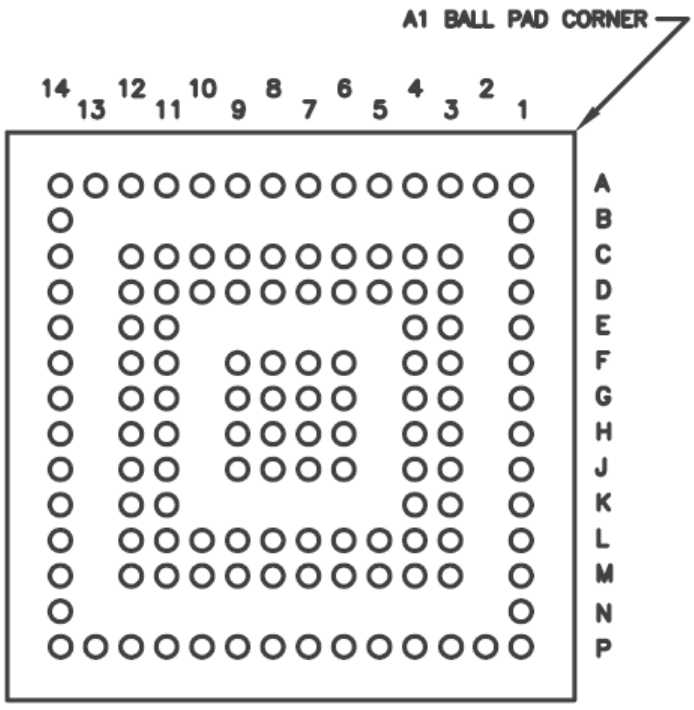
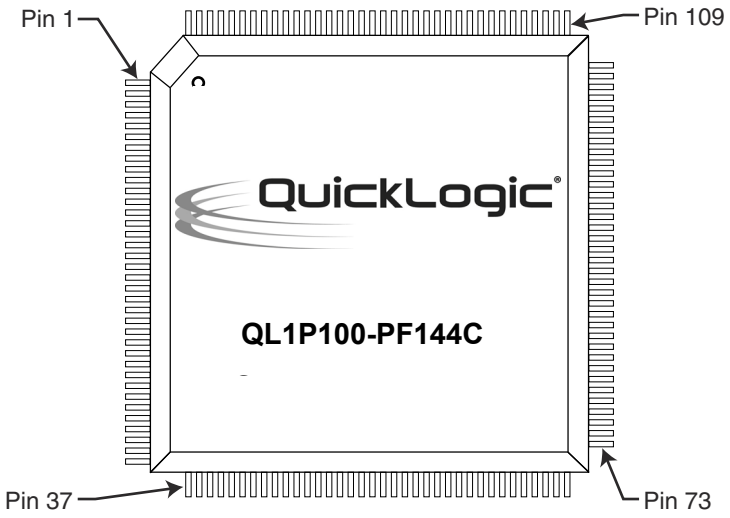
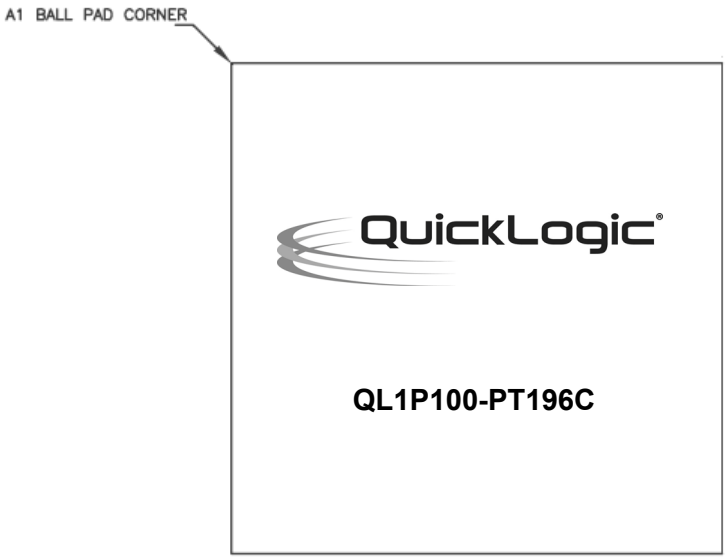


QL1P100 - 144 TQFP Pinout Diagram



QL1P100 - 196 TFBGA Pinout Diagram

Top



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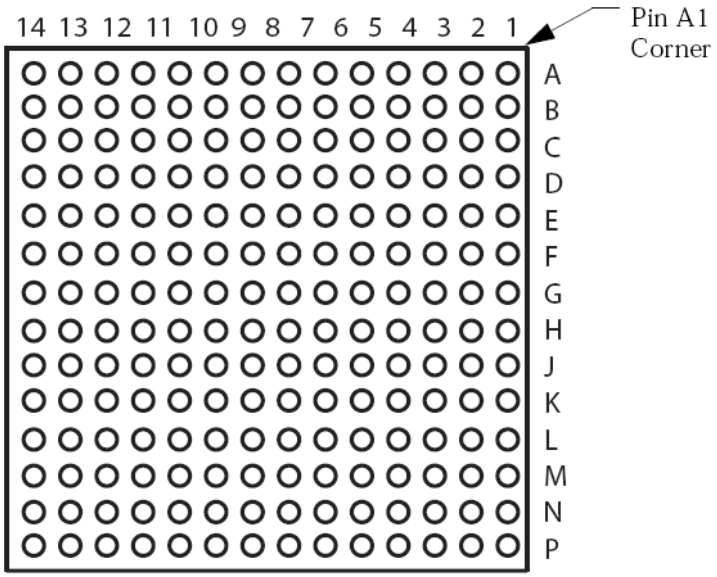
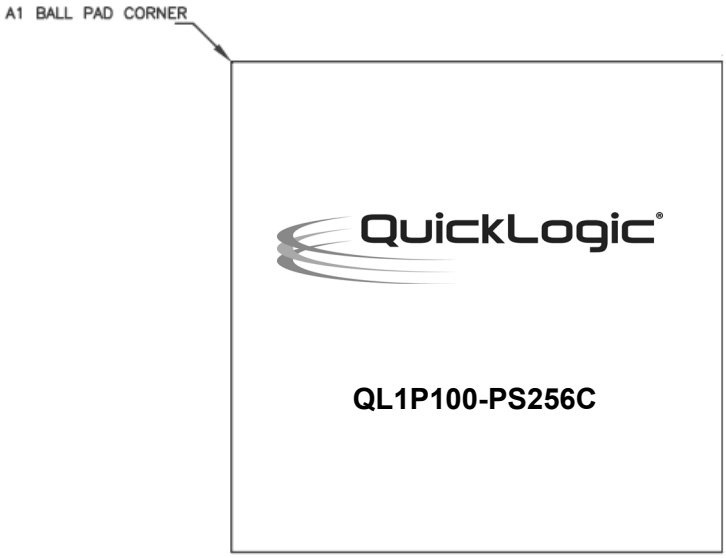


QL1P100 and QL1P300 - 256 LBGA Pinout Diagram

Top



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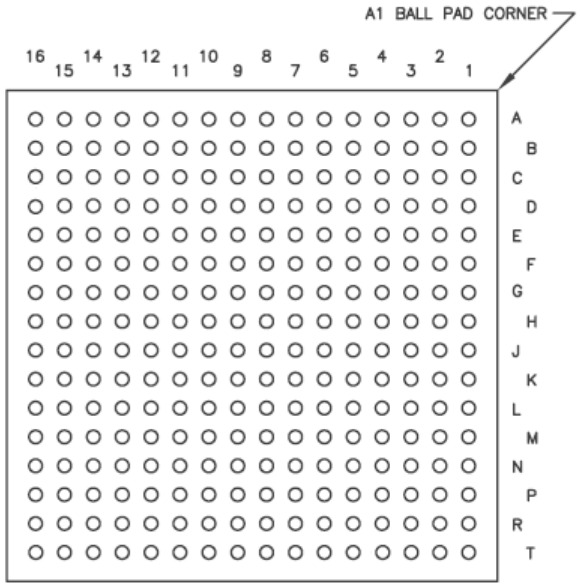
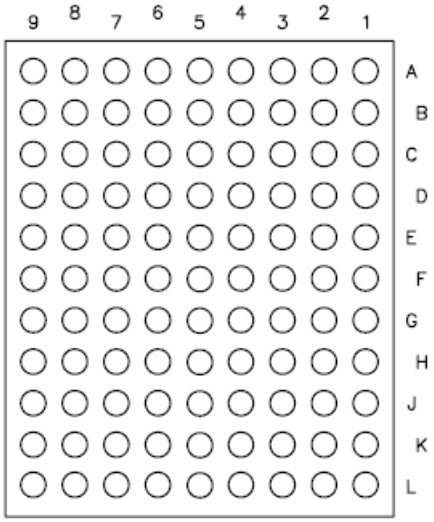


QL1P300 - 99 WLCSP Pinout Diagram

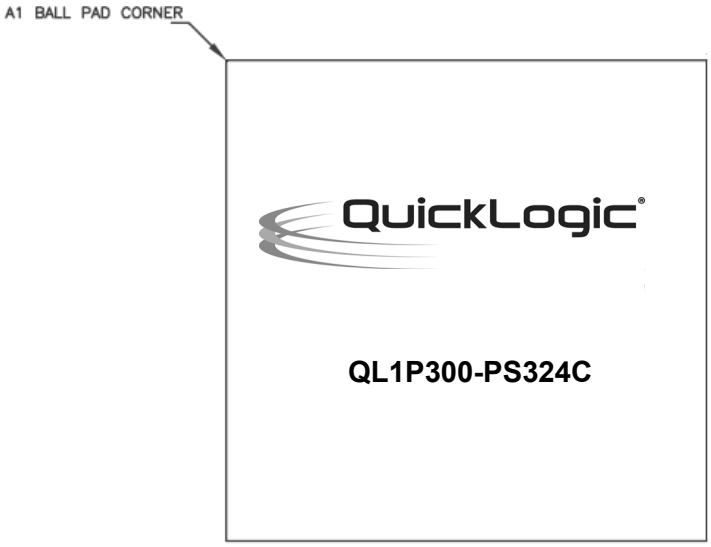
Top

Bottom



QL1P300 and QL1P1000 - 324 LBGA Pinout Diagram

Top



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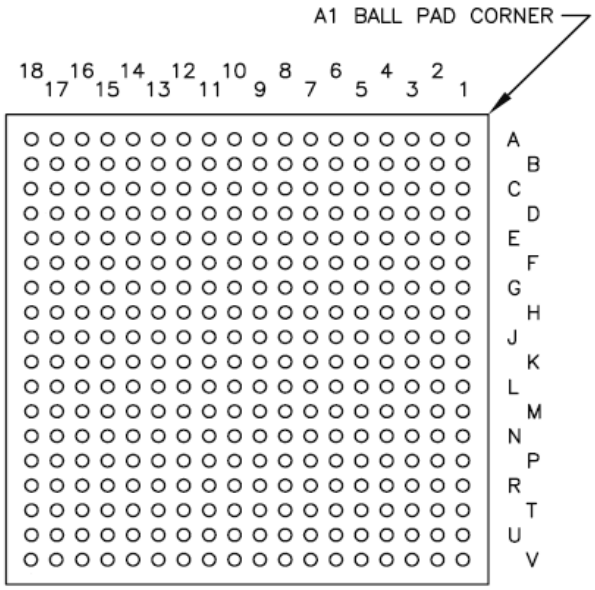
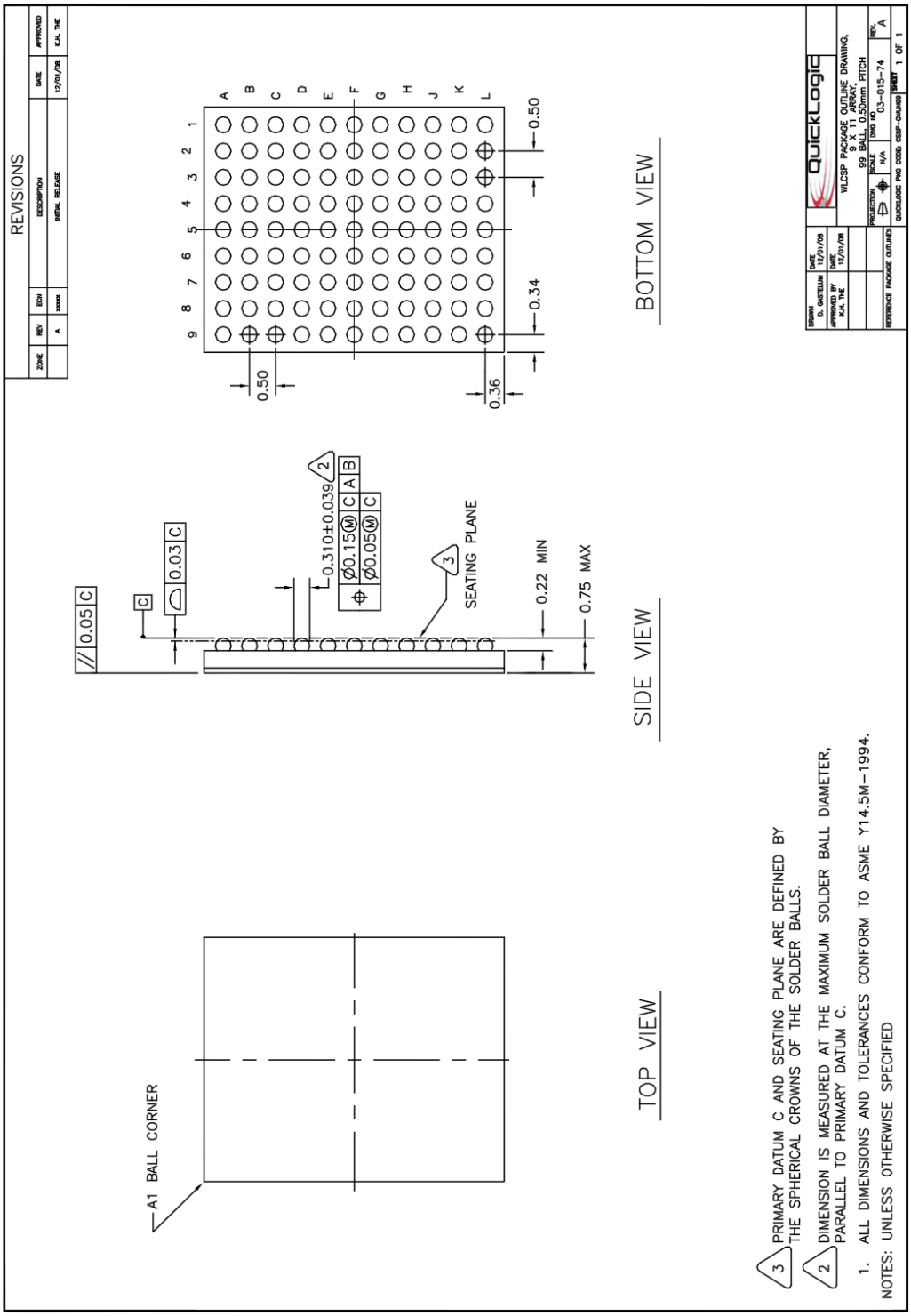
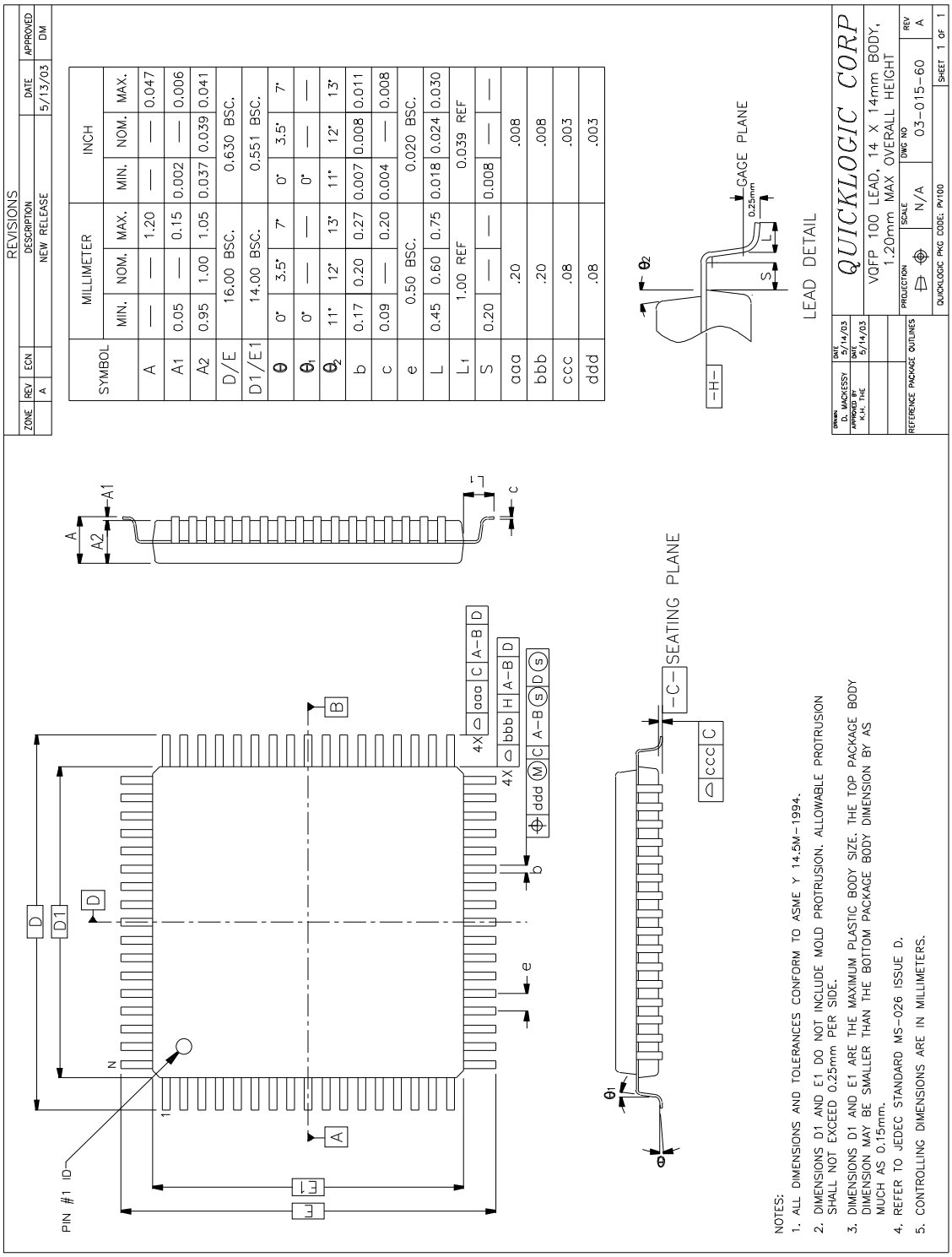


Package Mechanical Drawings

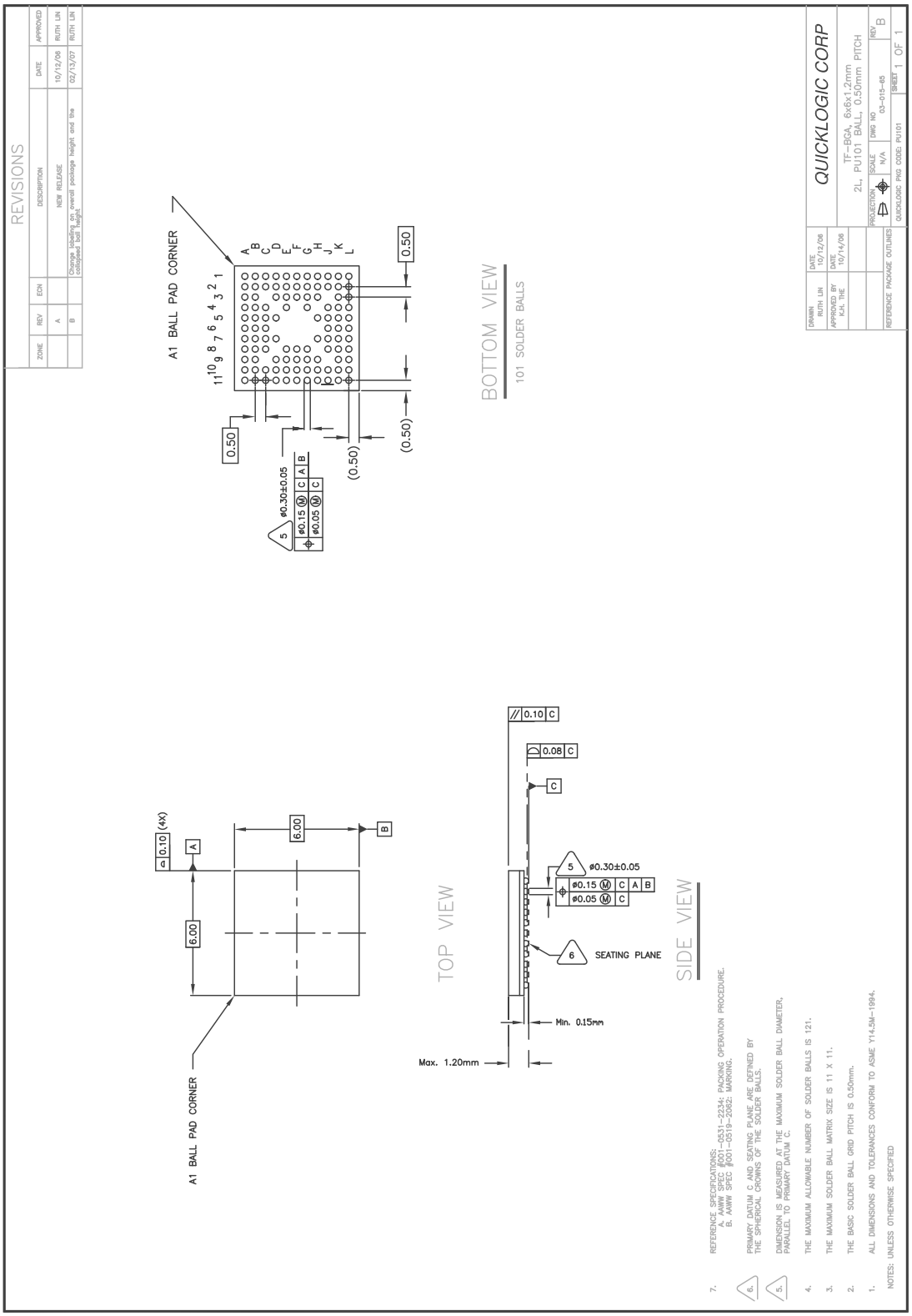
99 WLCSP Packaging Drawing



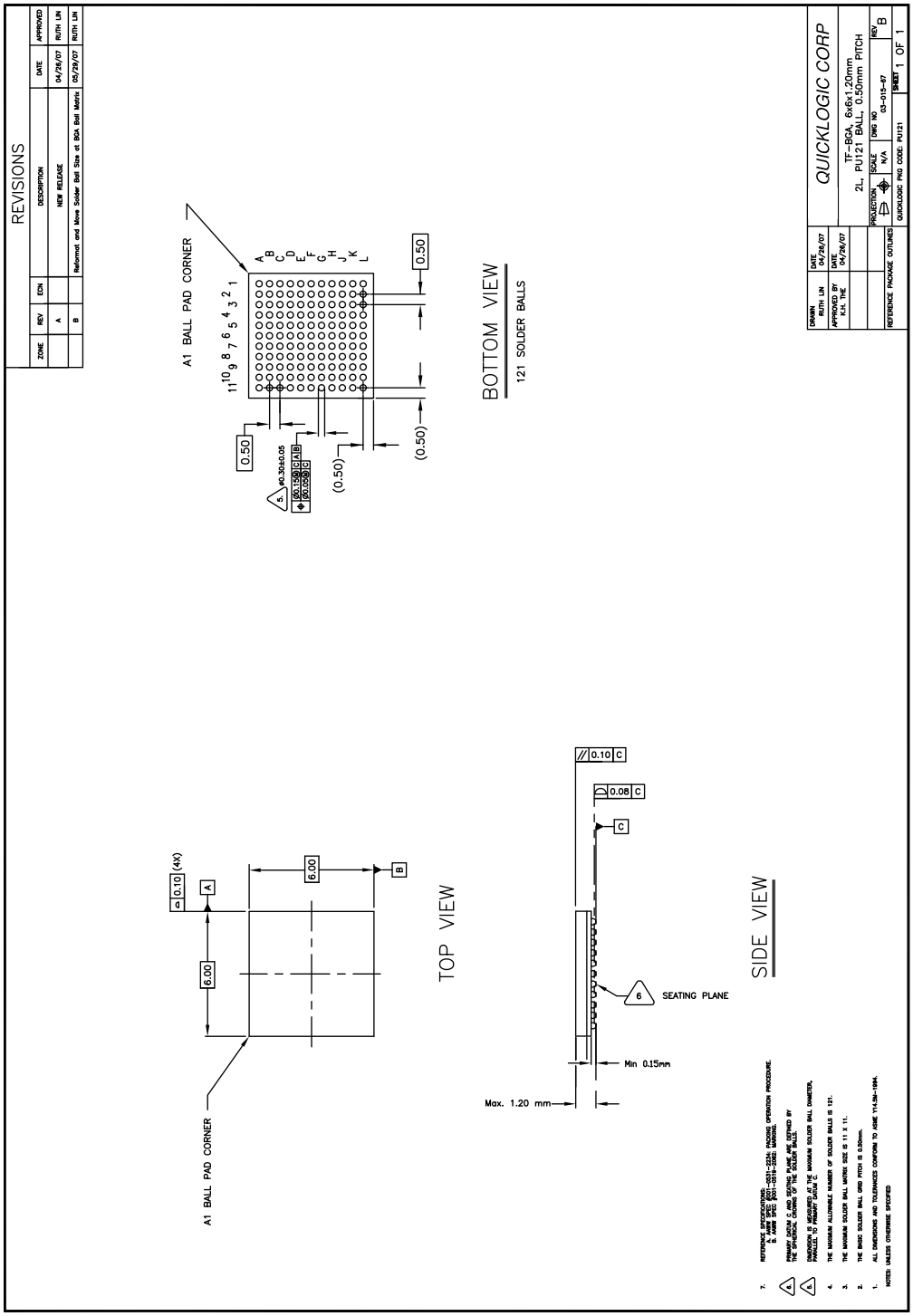
100 VQFP Packaging Drawing



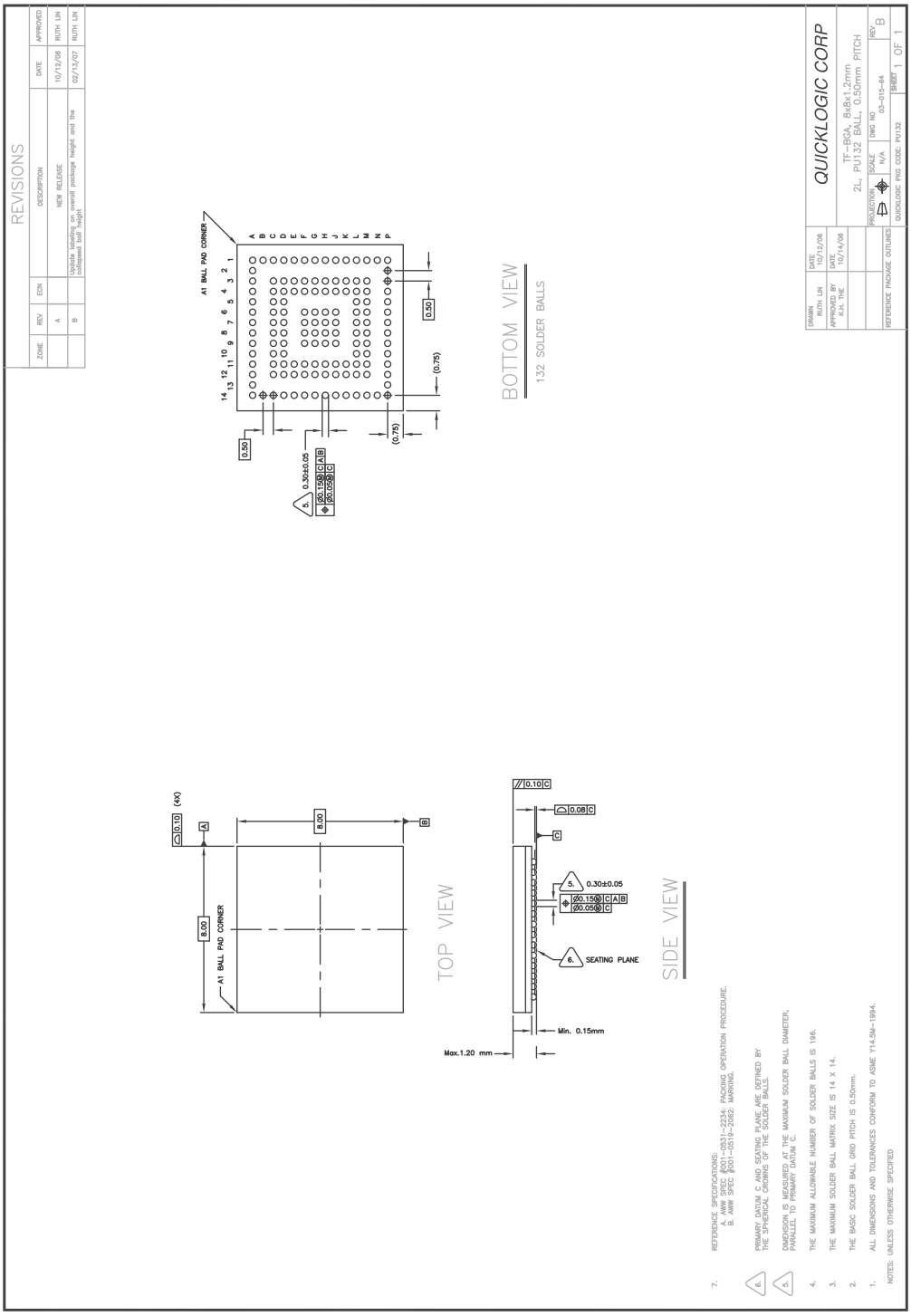
101 CTBGA Packaging Drawing



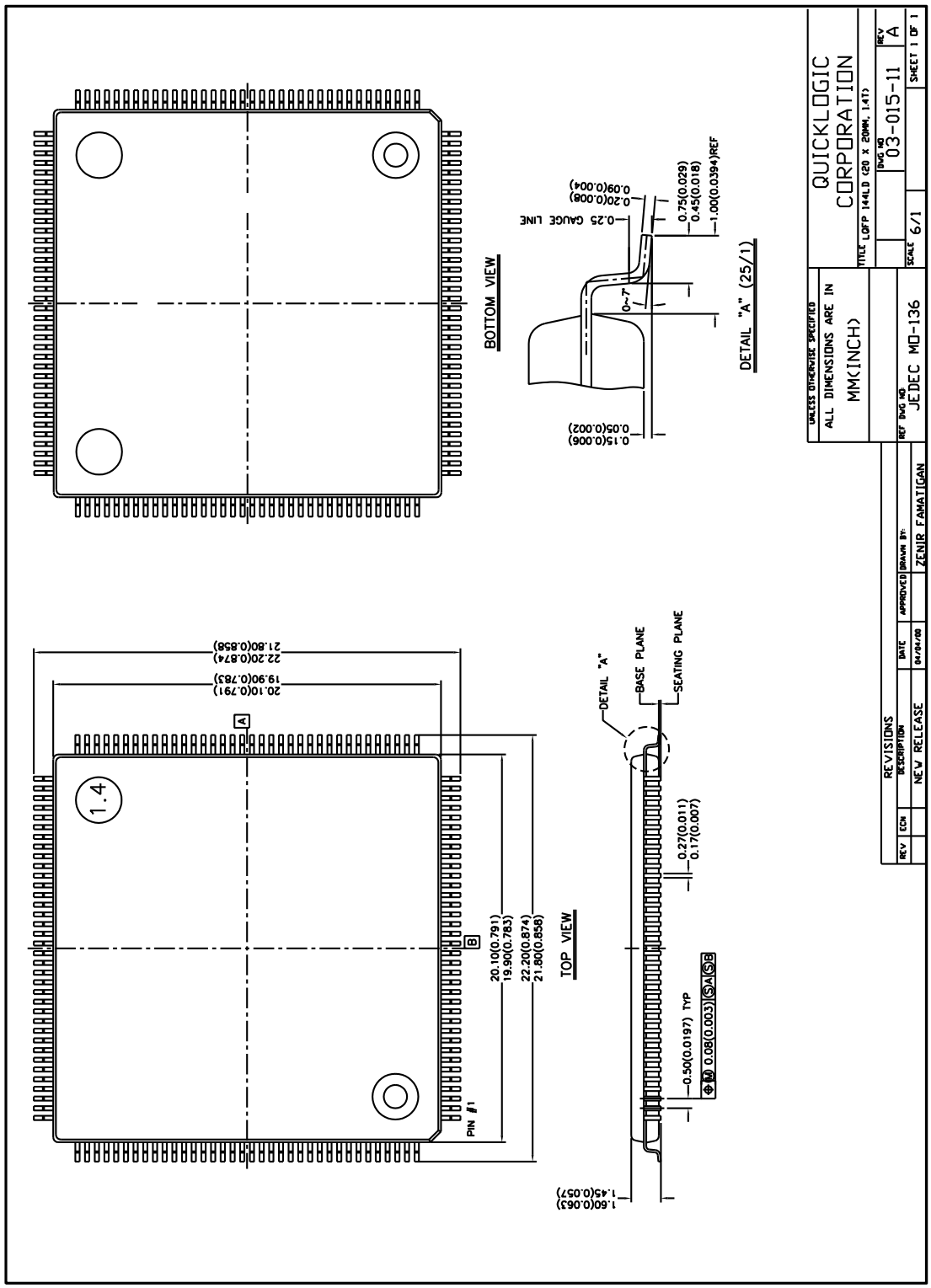
121 TFBGA Packaging Drawing



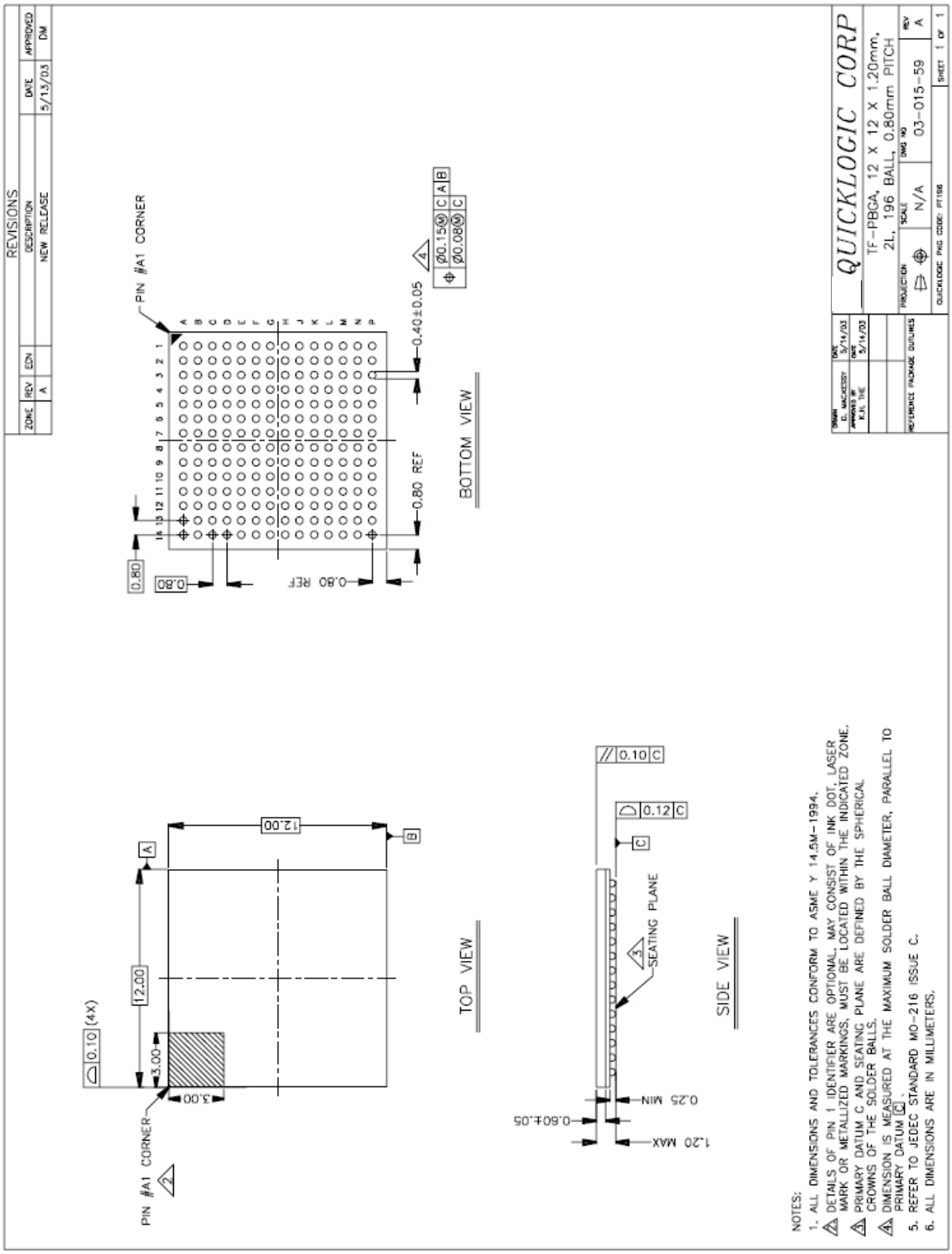
132 TFBGA Packaging Drawing



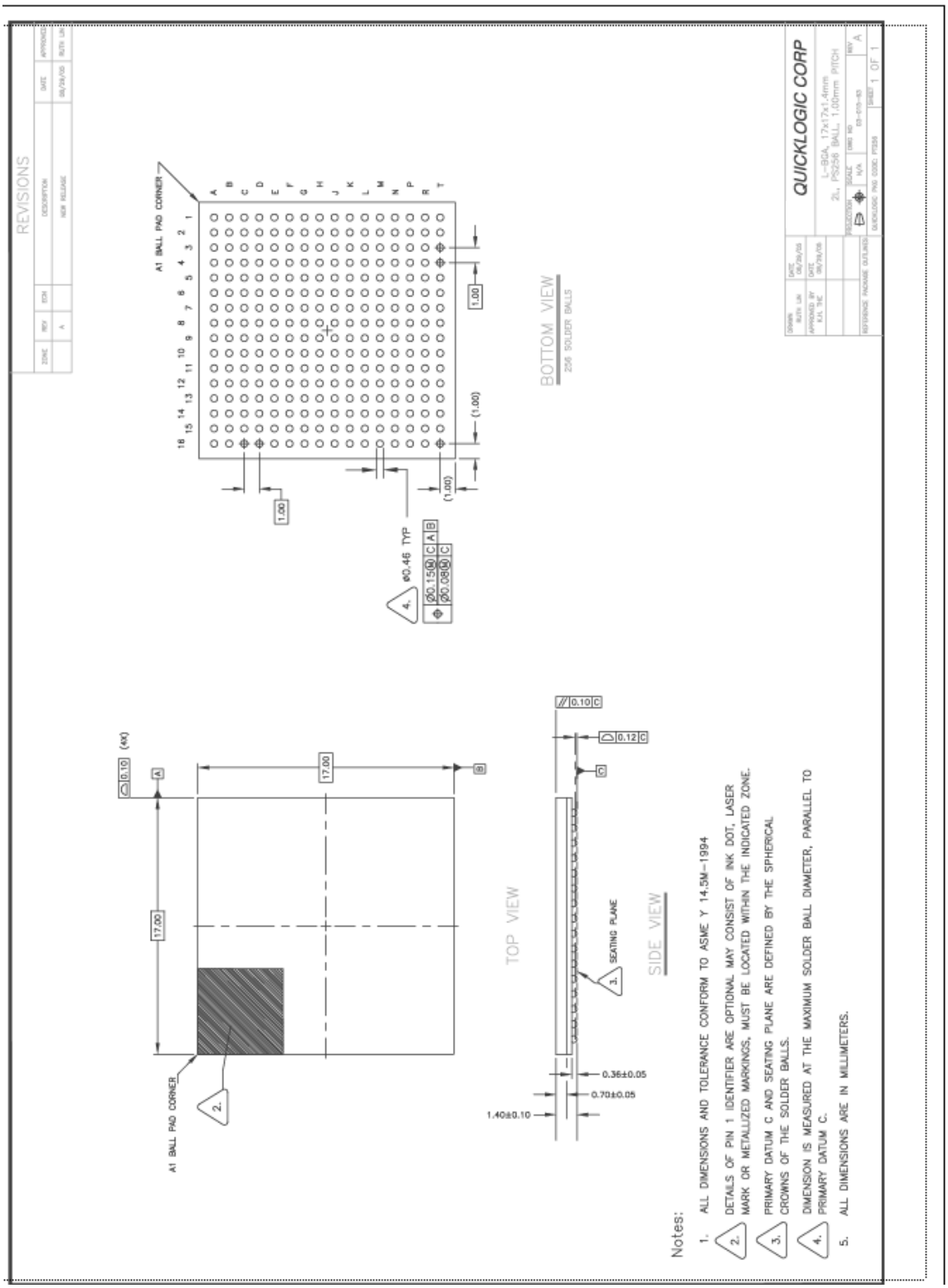
144 TQFP Packaging Drawing



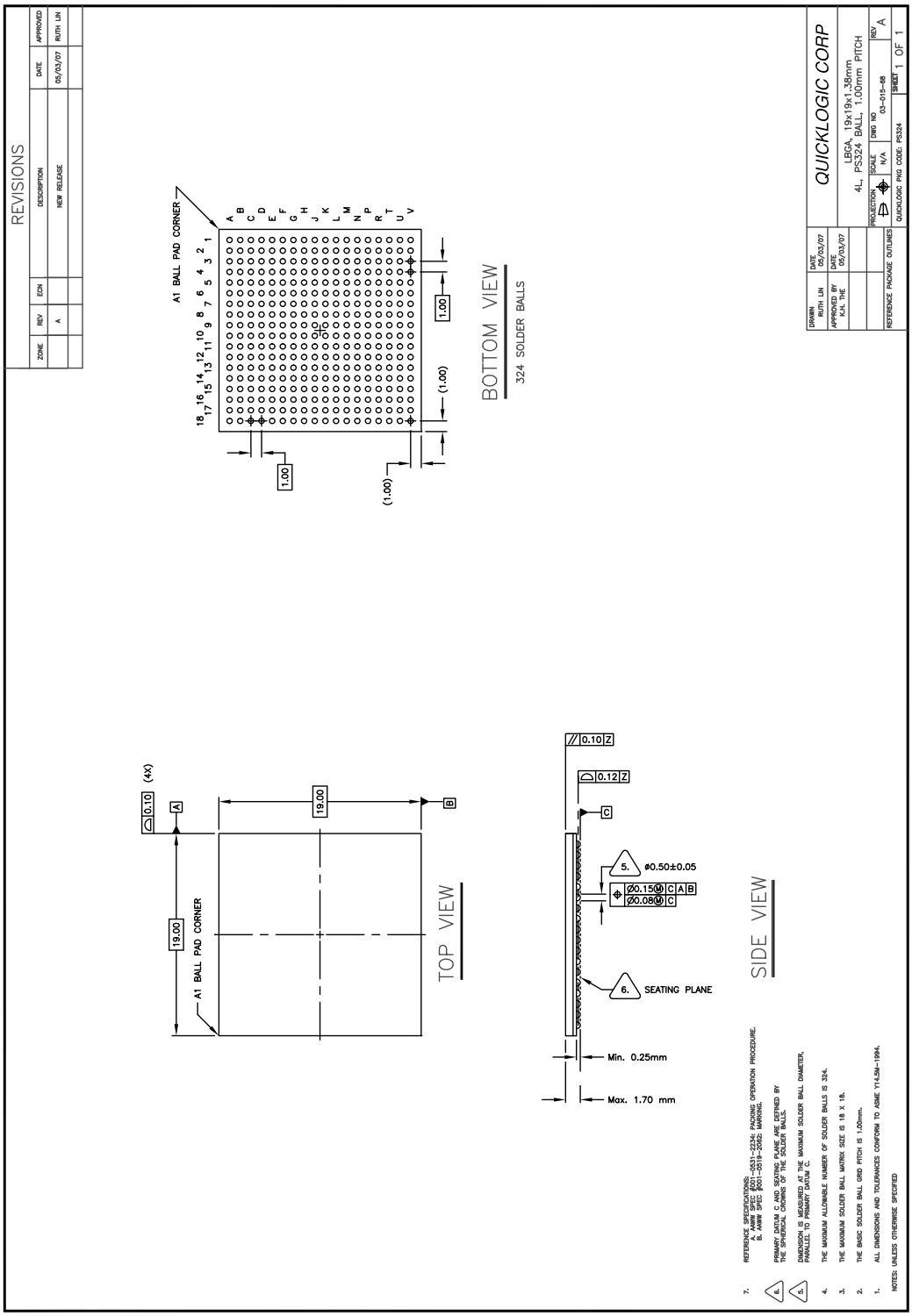
196 TFBGA Package Drawing



256 LBGA Packaging Drawing



324 LBGA Package Drawing



Packaging Information

The PolarPro Solution Platform family packaging information is shown in **Table 18**.

Table 18: PolarPro Solution Platform Family Packaging Options

Platform Information	Platform											
	QL8050			QL1P100			QL1P300			QL1P1000		
	Pin	Pb	Pb-Free	Pin	Pb	Pb-Free	Pin	Pb	Pb-Free	Pin	Pb	Pb-Free
Package Definitions[a]	100 VQFP (14 mm x 14 mm) Pitch - 0.50 mm	X	X	121 TFBGA (6 mm x 6 mm) Pitch - 0.50 mm		X	99 WLCSP Pitch - 0.50 mm		X	324 LBGA (19 mm x 19 mm) Pitch - 1.0 mm	X	X
	101 CTBGA (6 mm x 6 mm) Pitch - 0.50 mm		X	132 TFBGA (8 mm x 8 mm) Pitch - 0.50 mm		X	132 TFBGA (8 mm x 8mm) Pitch - 0.50 mm		X			
	144 TQFP (20 mm x 20 mm) Pitch - 0.50 mm	X	X	144 TQFP (20 mm x 20 mm) Pitch - 0.50 mm	X	X	256 LBGA (17 mm x 17 mm) Pitch - 1.0 mm	X	X			
	196 TFBGA (12 mm x 12 mm) Pitch - 0.80 mm	X	X	196 TFBGA (12 mm x 12 mm) Pitch - 0.80 mm	X	X	324 LBGA (19 mm x 19 mm) Pitch - 1.0 mm	X	X			
				256 LBGA (17 mm x 17 mm) Pitch - 1.0 mm	X	X						

a. CTBGA = ChipArray® Thin Ball Grid Array
TFBGA = Thin Profile Fine Pitch Ball Grid Array
LBGA = Low Profile Ball Grid Array
TQFP = Thin Quad Flat Pack
VQFP = Very Thin Quad Flat Pack
WLCSP = Wafer Level Chip Scale Packag

Ordering Information

PolarPro Solution Platform Customer Specific Standard Products (CSSPs) have assigned part numbers, contact your local sales representative for your specific CSSP number.

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Asia-sales@quicklogic.com
Japan-sales@quicklogic.com
Support: www.quicklogic.com/support
Internet: www.quicklogic.com

Revision History

Revision	Date	Originator and Comments
A	September 2007	Brian Faith and Kathleen Murchek
B	July 2008	Kathleen Murchek Updated Disclaimer, Copyright, Contact and Ordering information. Updated Figure 2 and Table 3. Removed 86-pin package.
C	January 2009	Jason Lew and Kathleen Murchek Added 99-pin WLCSP package.
D	May 2010	Kathleen Bylsma Updated GPIO pin description, removed pinout table, removed VEE trademark and updated contact info.

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