QuickLogic® PolarPro® II Device Data Sheet

Combining Low Power Programmable Fabric and Embedded SRAM

Device Highlights

Low Power Programmable Logic

- Up to 27 customizable building blocks (CBBs) for a detailed explanation of CBBs)
- Up to 27 kilobits of SRAM
- One user configurable clock manager (CCM)
- As low as 4.2 µA standby current
- 0.18 µm, six layer metal CMOS process
- 1.5 V or 1.8 V core voltage, 1.8/2.5/3.3 V drive capable I/Os
- Up to 103 I/Os available
- Up to 150,000 system gates
- Nonvolatile, instant-on
- IEEE 1149.1 boundary scan testing compliant

Embedded Dual-Port SRAM

- Up to four dual-port 4-kilobit and four 2-kilobit high performance SRAM blocks
- True dual-port capability for RAM and FIFOs
- Embedded synchronous/asynchronous FIFO controller
- Configurable and cascadable aspect ratio

Programmable I/O

- Individual programmable slew rate control
- Eight independent I/O banks capable of supporting multiple I/O standards in one device
- Bank programmable I/O standards: LVTTL, LVCMOS, LVCMOS18, and PCI

Advanced Clock Network

- Multiple low skew clock networks
  - 1 dedicated global clock network
  - 4 programmable global clock networks
- Quadrant-based segmentable clock networks
  - 20 quad clock networks per device
  - 4 quad clock networks per quadrant
  - 1 dedicated clock network per quadrant
- One user Configurable Clock Manager (CCM)

Very Low Power (VLP) Mode

- QuickLogic PolarPro II device has a special VLP pin which can enable a low power sleep mode that significantly reduces the overall power consumption of the device by placing the device in standby
- Enter/exit VLP mode from/to normal operation in less than 10 µs (typical)

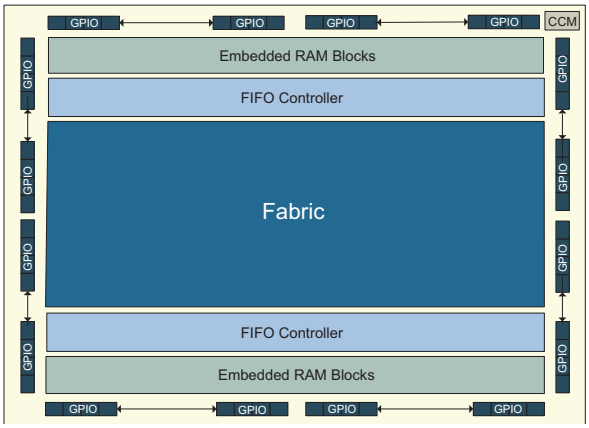
JTAG

QuickLogic PolarPro II family of solution platforms supports IEEE 1149.1 boundary scan or post-manufacturing testability. External access to this feature can be completely disabled.

Security Links

There are several security links to disable JTAG access to the device. Programming these optional links completely disables access to the device from the outside world and provides an extra level of design security not possible in SRAM-based FPGAs.

Figure 1: QuickLogic PolarPro II Block Diagram



Ultra-Low Power FPGA Combining Performance, Density, and Embedded SRAM

Table 1 summarizes the PolarPro II device family features.

Table 1: PolarPro II Device QL2P150

Features		QL2P150
Max Gates		150,000
Logic Cells		864
RAM Modules		8
FIFO Controllers		8
RAM bits		27,648
CCMs		1
Max I/O per Package	144 VFBGA (0.4 mm pitch)	103
	121 TFBGA (0.5 mm pitch)	81
	64 WLCSP (0.4 mm pitch)	41

Process Data

The QuickLogic PolarPro II is fabricated on a 0.18µ, six layer metal CMOS process. The core voltage is 1.5 V or 1.8 V. The I/O voltage input tolerance and output drive can be set as 1.8 V, 2.5 V, and 3.3 V.

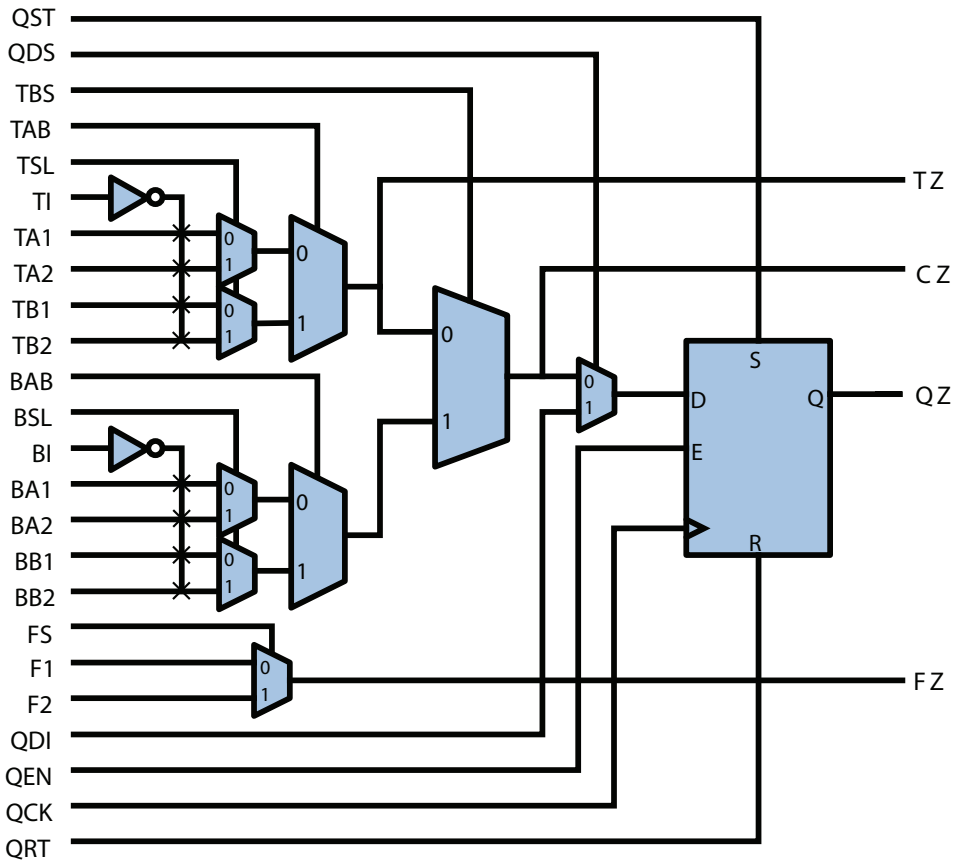
Programmable Logic Architectural Overview

The QuickLogic PolarPro II logic cell structure presented in **Figure 2** is a single register, multiplexer-based logic cell. It is designed for wide fan-in and multiple, simultaneous output functions. The cell has a high fan-in, fits a wide range of functions with up to 24 simultaneous inputs (including register control lines), and four outputs (three combinatorial and one registered). The high logic capacity and fan-in of the logic cell accommodates many user functions with a single level of logic delay.

The QuickLogic PolarPro II logic cell can implement:

- Two independent 3-input functions
- Any 4-input function
- 8 to 1 mux function
- Independent 2 to 1 mux function
- Single dedicated register with clock enable, active high set and reset signals
- Direct input selection to the register, which allows combinatorial and register logic to be used separately
- Combinatorial logic that can also be configured as an edge-triggered master-slave D flip-flop

Figure 2: PolarPro II Logic Cell



RAM Modules

The PolarPro II QL2P150 device has four 4-kilobit (4608 bits) as shown in **Figure 3**, and four 2-kilobit (2304) RAM blocks as shown in **Figure 4**.

The RAM features include:

- Independently configurable read and write data bus widths
- Independent read and write clocks
- Maximum of two RAM blocks can be concatenated horizontally or vertically
  - 4 kilobits for two 2-kilobit RAM blocks and 8 kilobits for two 4-kilobit RAM blocks
- Write byte enables
- Selectable pipelined or non-pipelined read data
- True dual-port RAM functionality
- Clock disabling during idle operation

Figure 3: 4-Kilobit Dual-Port RAM Block

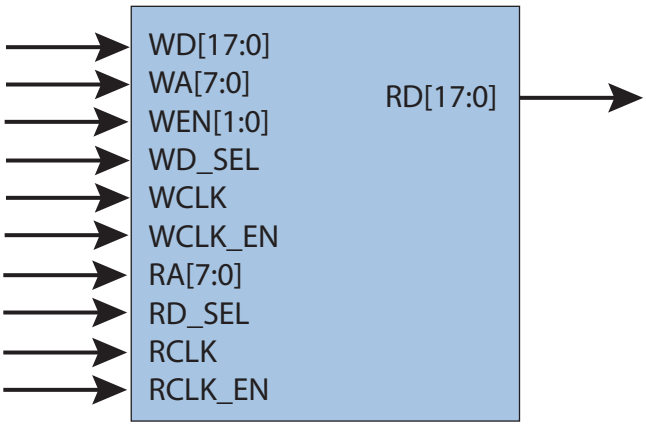


Figure 4: 2-Kilobit Dual-Port RAM Block

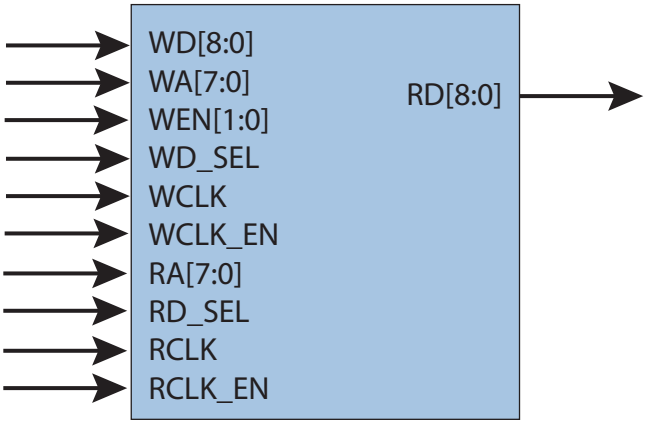


Table 2 describes the RAM interface signals.

Table 2: RAM Interface Signals

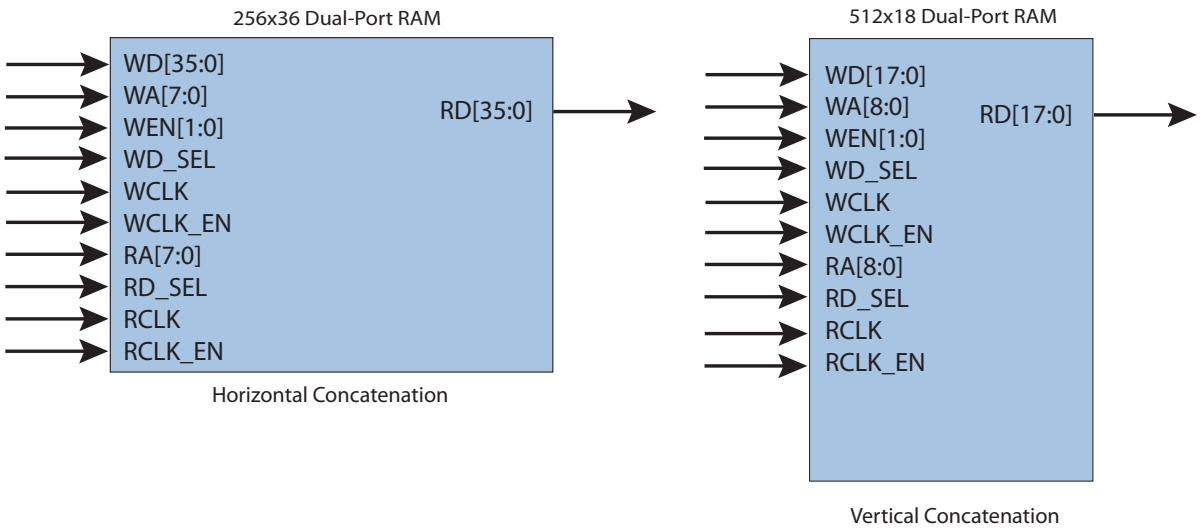
Signal Name	Function
Inputs	
WD	Write Data
WA	Write Address
WEN	Write Enable
WD_SEL	Write Chip Select
WCLK	Write Clock
WCLK_EN	Write Clock Enable
RA	Read Address
RD_SEL	Read Chip Select
RCLK	Read Clock
RCLK_EN	Read Clock Enable
Output	
RD	Read Data

The read and write data buses of a RAM block can be arranged to variable bus widths. The bus widths can be configured using the RAM Wizard available in QuickWorks, QuickLogic's development software. The selection of the RAM depth and width determines how the data is addressed.

The RAM blocks also support data concatenation. Designers can cascade multiple RAM modules to increase the depth or width by connecting corresponding address lines together and dividing the words between modules. Generally, this requires the use of additional programmable logic resources. However, when concatenating only two 4-kilobit RAM blocks or two 2-kilobit RAM blocks, they can be concatenated horizontally or vertically without using any additional programmable fabric resources.

For example, two internal 4-kilobit dual-port RAM blocks can be concatenated vertically to create a 512x18 RAM block or horizontally to create a 256x36 RAM block. **Figure 5** displays a block diagram of 4-kilobit RAM blocks horizontal and vertical concatenation.

Figure 5: 4-Kilobit Horizontal and Vertical Concatenation Examples



For example, two internal 2-kilobit dual-port RAM blocks can be concatenated vertically to create a 256x18 RAM block or horizontally to create a 128x36 RAM block. **Figure 6** displays a block diagram of 2-kilobit RAM blocks horizontal and vertical concatenation.

Figure 6: 2-Kilobit Horizontal and Vertical Concatenation Examples

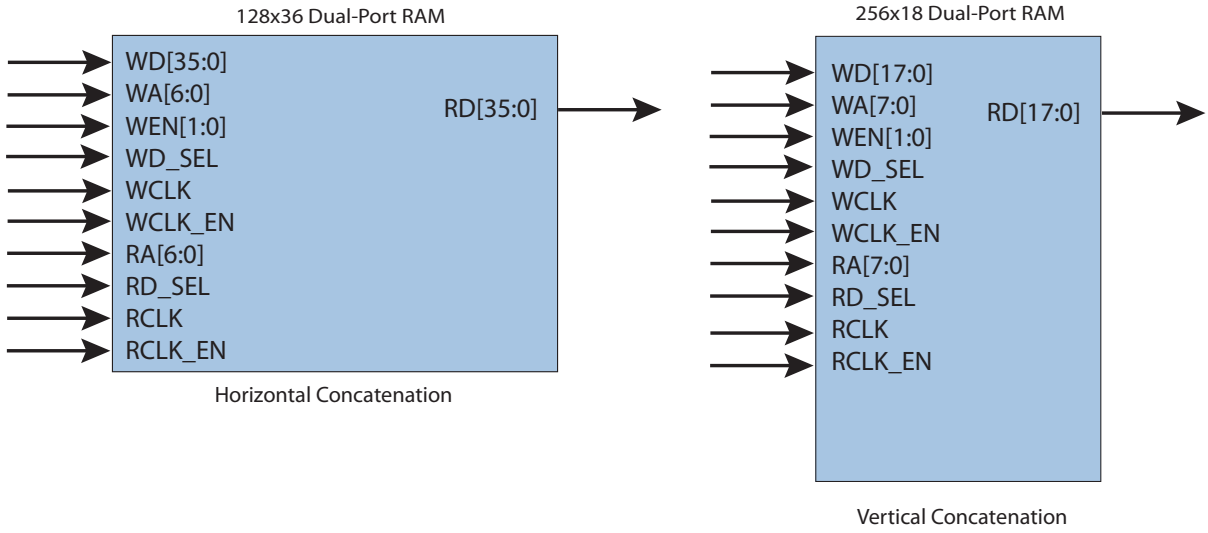


Table 3 shows the various RAM configurations supported by the PolarPro II 4-kilobit RAM modules.

Table 3: Available 4-Kilobit RAM Configurations

Device	Number of RAM Blocks	Depth	Width	Description
QL2P150	1	256	1-18	No concantenation
	1	512	1-9	No concantenation
	2	256	1-36	Horizontal concantenation
	2	512	1-18	Vertical concantenation
	2	1024	1-9	Vertical concantenation

Table 4 shows the various RAM configurations supported by the PolarPro II 2-kilobit RAM modules.

Table 4: Available 2-Kilobit RAM Configurations

Device	Number of RAM Blocks	Depth	Width	Description
QL2P150	1	128	1-18	No concantenation
	1	256	1-9	No concantenation
	2	128	1-36	Horizontal concantenation
	2	256	1-18	Vertical concantenation
	2	512	1-9	Vertical concantenation

True Dual-Port RAM

PolarPro II dual-port RAM modules can also be concatenated to generate true dual-port RAMs. The true dual-port RAM module's Port1 and Port2 have completely independent read and write ports, and separate read and write clocks. This allows Port1 and Port2 to have different data widths and clock domains. It is important to note that there is no circuitry preventing a write and read operation to the same address space at the same time. Therefore, it is up to the designer to ensure that the same address is not read from and written to simultaneously, otherwise the data is considered invalid. Likewise, the same address must not be written to from both ports at the same time. However, it is possible to read from the same address.

Figure 7 shows an example of a 512x18 true dual-port RAM.

Figure 7: 512x18 4-Kilobit True Dual-Port RAM Block

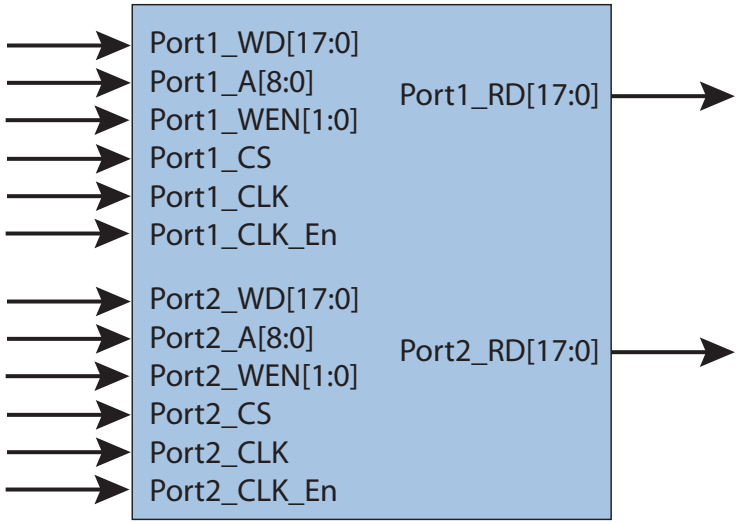


Figure 8 shows an example of a 256x18 true dual-port RAM.

Figure 8: 256x18 2-Kilobit True Dual-Port RAM Block

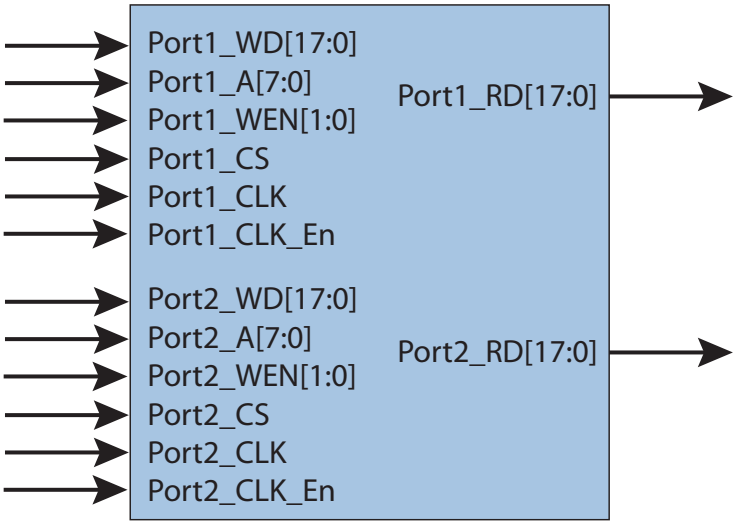


Table 5 describes the true dual-port RAM interface signals.

Table 5: True Dual-Port RAM Interface Signals

Port	Signal Name	Function
Port1	**Inputs**	
	Port1_WD	Write Data
	Port1_A	Write Address
	Port1_WEN	Write Enable
	Port1_CS	Chip Select
	Port1_CLK	Clock
	Port1_CLK_En	Clock Enable
	Output	
	Port1_RD	Read Data
Port2	**Inputs**	
	Port2_WD	Write Data
	Port2_A	Write Address
	Port2_WEN	Write Enable
	Port2_CS	Chip Select
	Port2_CLK	Clock
	Port2_CLK_En	Clock Enable
	Output	
	Port2_RD	Read Data

Table 6 lists the 4-kilobit true dual-port RAM configurations that are available.

Table 6: Available 4-Kilobit True Dual-Port RAM Configurations

Device	Depth	Width
QL2P150	512	1-18
	1024	1-9

Table 7 lists the 2-kilobit true dual-port RAM configurations that are available.

Table 7: Available 2-Kilobit True Dual-Port RAM Configurations

Device	Depth	Width
QL2P150	256	1-18
	512	1-9

Embedded FIFO Controllers

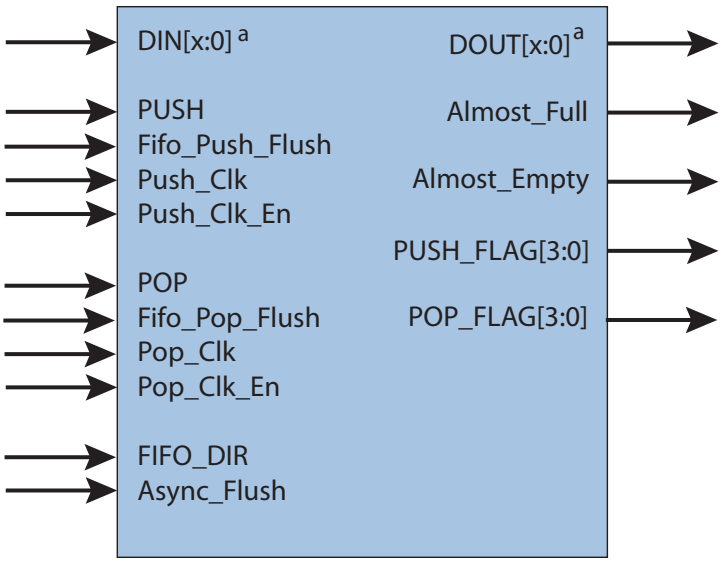
Each RAM block can be implemented as a synchronous or asynchronous FIFO. There are built-in FIFO controllers that allow for varying depths and widths without requiring programmable fabric resources.

The PolarPro II FIFO controller features include:

- x9, x18 and x36 data bus widths
- Independent PUSH and POP clocks
- Independent programmable data width on PUSH and POP sides
- Configurable synchronous or asynchronous FIFO operation
- 4-bit PUSH and POP level indicators to provide FIFO status outputs for each port
- Pipelined read data to improve timing
- Switchable clock domain between PUSH and POP side during asynchronous operation
- Clock disabling during idle operation
- Asynchronous reset (apart from the synchronous FLUSH) going to the pointers

Figure 9 shows an example a FIFO module.

Figure 9: FIFO Module



a. x = {1,2,3,....35}.

Table 8 lists the FIFO configurations that are available.

Table 8: Available FIFO Configurations

Device	Number of RAM Blocks	Depth	Supported Widths
QL2P150	1 (2-kilobit RAM block)	128	1-18 bits
	1 (2-kilobit RAM block)	256	1-9 bits
	2 (2-kilobit RAM block)	128	1-36 bits
	2 (2-kilobit RAM block)	256	1-18 bits
	2 (2-kilobit RAM block)	512	1-9 bits
	1 (4-kilobit RAM block)	256	1-18 bits
	1 (4-kilobit RAM block)	512	1-9 bits
	2 (4-kilobit RAM block)	256	1-36 bits
	2 (4-kilobit RAM block)	512	1-18 bits
	2 (4-kilobit RAM block)	1024	1-9 bits

Table 9 lists the FIFO controller interface signals.

Table 9: FIFO Interface Signals

Signal Name	Width (bits)	Direction	Function
PUSH Signals			
DIN	1 to 36	I	Data bus input
PUSH	1	I	Initiates a data push
Fifo_Push_Flush	1	I	Empties the FIFO
Push_Clk	1	I	Push data clock
Push_Clk_En	1	I	Push clock enable
POP Signals			
DOUT	1 to 36	O	Data bus output
POP	1	I	Initiates a data pop
Fifo_Pop_Flush	1	I	Empties the FIFO
Pop_Clk	1	I	Pop data clock
Pop_Clk_En	1	I	Pop clock enable
Common PORT Signals			
Fifo_Dir	1	I	Push-Pop domain switching
Async_Flush	1	I	Asynchronous input to flush FIFO
Status Flags			
Almost_Full	1	O	Asserted when FIFO has one location available
Almost_Empty	1	O	Asserted when FIFO has one location used
PUSH_FLAG	4	O	FIFO PUSH level indicator
POP_FLAG	4	O	FIFO POP level indicator

Table 10 and **Table 11** highlight the corresponding FIFO level indicator for each 4-bit value of the PUSH_FLAG and POP_FLAG outputs.

Table 10: FIFO PUSH Level Indicator Values

Value	Status
0000	Full
0001	Empty
0010	Room for more than one-half
0011	Room for more than one-forth
0100	Room for less than one-forth to 64[a]
1010	Room for 32 to 63[a]
1011	Room for 16 to 31
1100	Room for 8 to 15
1101	Room for 4 to 7
1110	Room for 2 to 3
1111	Room for 1
Others	Reserved

a. For a FIFO depth of 256, Value 0100 will not be asserted. The PUSH flag will shift directly from 0011 to 1010 as data is pushed. For a FIFO depth of 128, Values 0100 and 1010 will not be asserted. The PUSH flag will shift directly from 0011 to 1011 as data is pushed.

Table 11: FIFO POP Level Interface Signals

Value	Status
0000	Empty
0001	1 entry in FIFO
0010	At least 2 entries in FIFO
0011	At least 4 entries in FIFO
0100	At least 8 entries in FIFO
0101	At least 16 entries in FIFO
0110	At least 32 entries in FIFO[a]
1000	64 entries to less than one-forth full[a]
1101	One-forth or more full
1110	One-half or more full
1111	Full
Others	Reserved

a. For a FIFO depth of 256, Value 1000 will not be asserted. The POP Flag will shift directly from 1101 to 0110 as data is popped. For a FIFO depth of 128, Values 1000 and 0110 will not be asserted. The POP flag will shift directly from 1101 to 0101 as data is popped.

PUSH-POP Domain Switching

During asynchronous operation, the FIFO works in a half-duplex manner, meaning PUSH on one clock domain and POP on the other clock domain. To provide each domain the PUSH and POP capability, a DIR port is added to choose what function each clock domain will have. The DIR port determines the functions of P1 and P2, and the clock assigned to PORT1 and PORT2 of the FIFO. After the direction switches, the FIFO pointers must be reset.

Figure 10 shows the PUSH-POP domain switching operation.

Figure 10: PUSH-POP Domain Switching

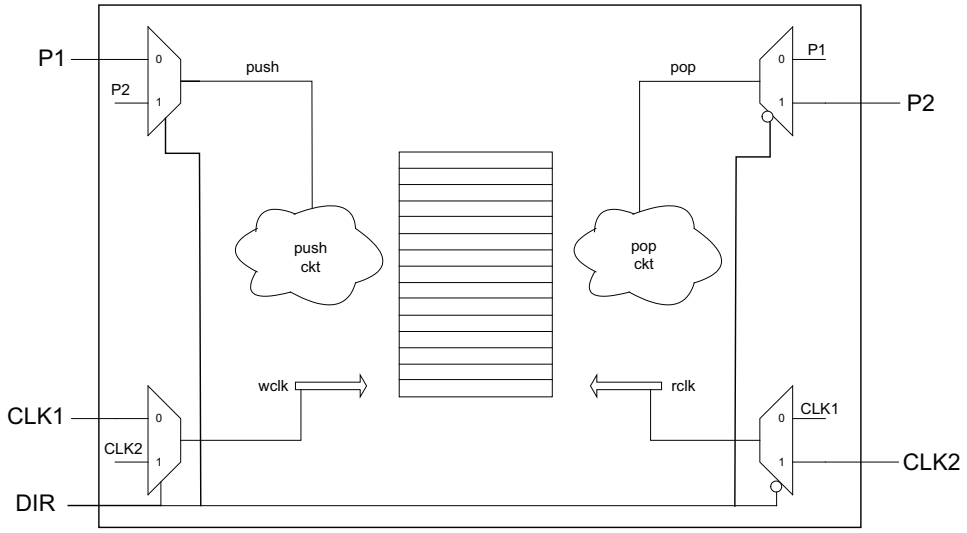


Table 12 shows the PUSH-POP direction switching.

Table 12: PUSH-POP Direction Switching

DIR	Direction
0	CLK1/P1 PUSH, CLK2/P2 POP
1	CLK1/P1 POP, CLK2/P2 PUSH

FIFO Synchronous Flush Procedure

Both PUSH and POP domains are provided with a flush input signal synchronized to their respective clocks. When a flush is triggered from one side of the FIFO, the signal propagates and re-synchronizes internally to the other clock domain. During a flush operation, the values of the FIFO flags are invalid for a specific number of cycles (see **Figure 11** and **Figure 12**).

As shown in **Figure 11**, when the **Fifo_Push_Flush** asserts, the **Almost_Full** and **PUSH_FLAG** signals become invalid until the FIFO can flush the data with regards to the Push clock domain as well as the Pop clock domain. After the **Fifo_Push_Flush** is asserted, the next rising edge of the Pop clock starts the Pop flush routine.

Figure 11 illustrates a FIFO Flush operation. After the **Fifo_Push_Flush** is asserted at 2 (**PUSH_Clk**), four POP clock cycles (12 through 15) are required to update the **POP_FLAG**, and **PUSH_FLAG** signals. The **Almost_Empty** signal is asserted to indicate that the push flush operation has been completed. On the following rising edge of the **PUSH_Clk** (8), the **PUSH_FLAG** is accordingly updated to reflect the successful flush operation.

Figure 11: FIFO Flush from PUSH Side

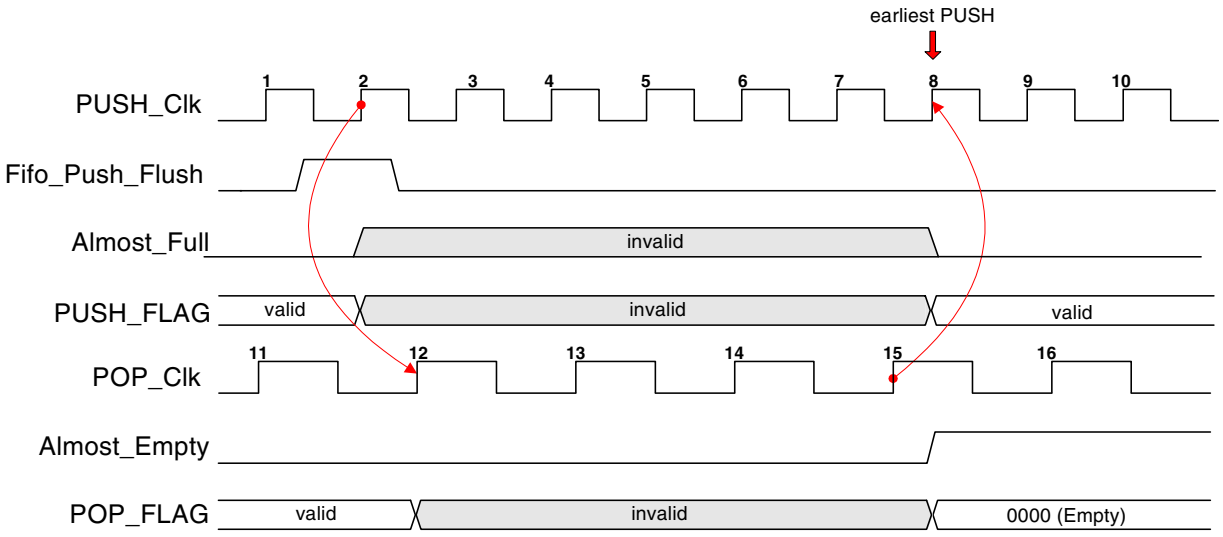


Figure 12 illustrates a POP flush operation. After the **Fifo_Pop_Flush** is asserted at 2 (**POP_Clk**), four PUSH clock cycles (12 through 15) are required to update the **POP_FLAG**, and **PUSH_FLAG** signals. The **Almost_Empty** signal is asserted to indicate that the pop flush operation has been completed. On the following rising edge of the **POP_Clk** (8), the **POP_FLAG** is updated accordingly to reflect the successful flush operation.

Figure 12: FIFO Flush from POP Side

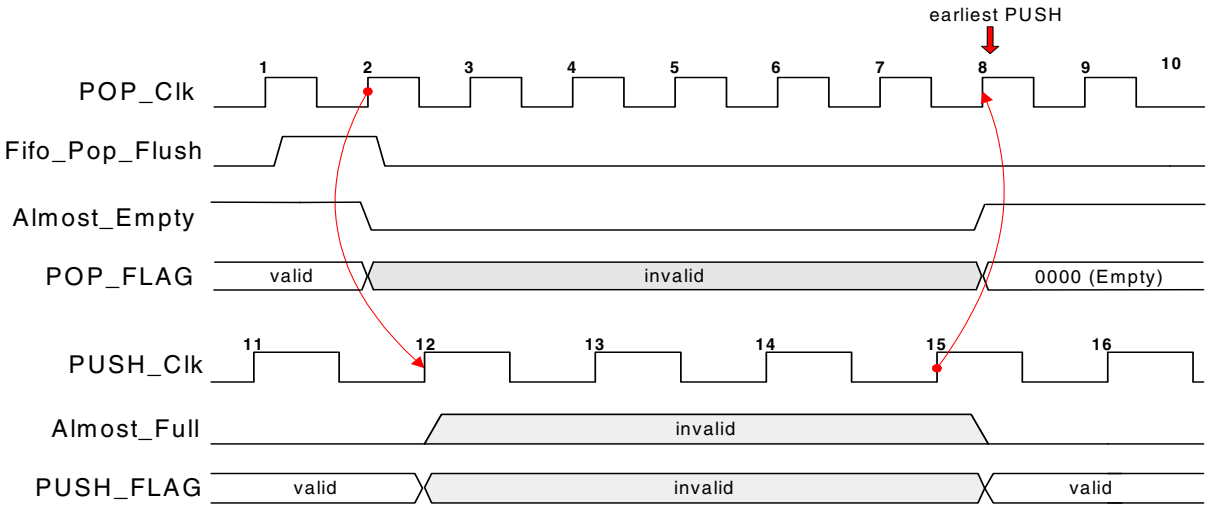


Figure 11 and **Figure 12** are only true for this particular PUSH-POP clock frequency combination. The clock frequency and phase difference between POP_Clk and PUSH_Clk can cause an additional flush delay of one clock cycle in either domain because of the asynchronous relationship between the two clocks.

Asynchronous Flush

Apart from the synchronous flush controls, an asynchronous flush is provided through the port ASYNC_FLUSH. Assertion of this signal flushes the FIFO PUSH and POP pointers.

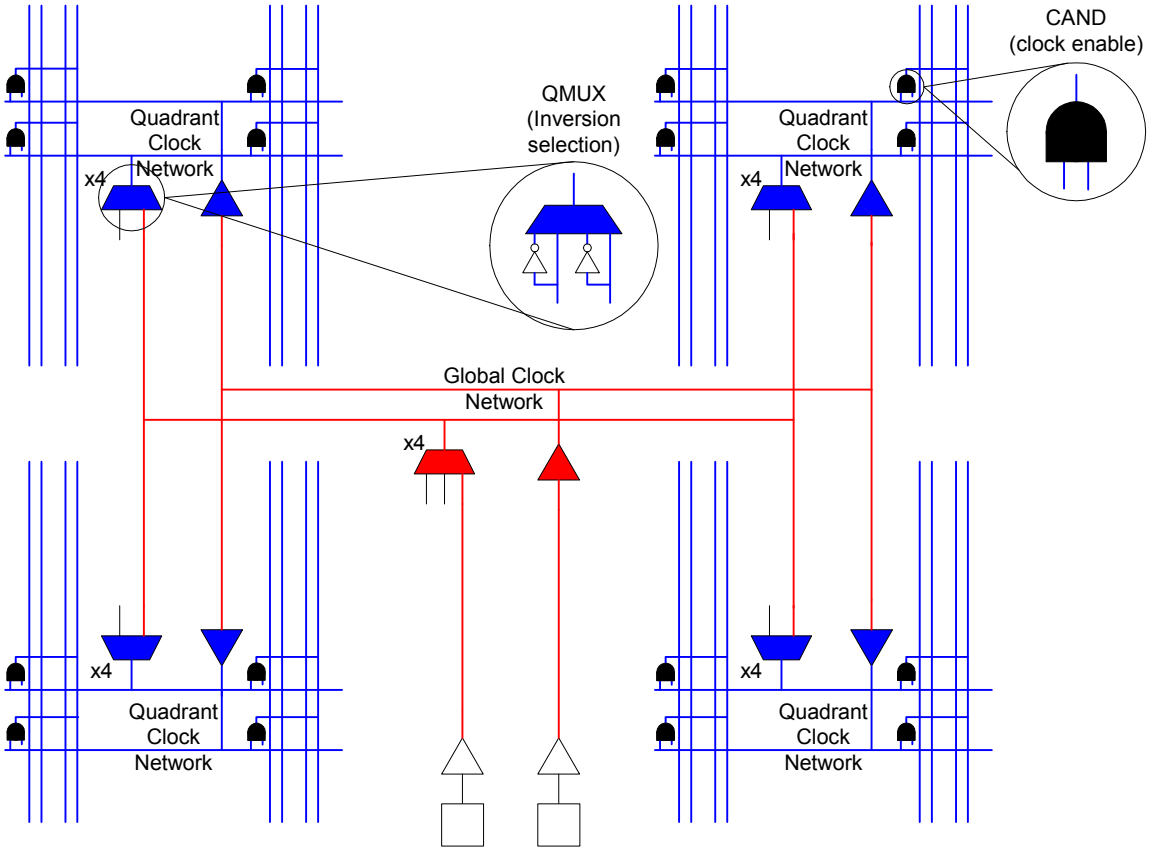
QL2P150 Clock Network Architecture

Clock Network Architecture

The PolarPro II clock network architecture consists of a 2-level H-tree network as shown in **Table 13**. The first level of each clock tree spans from the clock input pad to the global clock network and to the center of each quadrant of the chip. The second level spans from the quadrant clock network to every logic cell inside that quadrant. There are five global clocks in the global clock network, and five quadrant clocks in each quadrant clock network. All global clocks drive the quadrant clock network inputs.

The quadrant clock network passes either the original input clock or an inverted version of the input clock to the column clock buffer. The column clock buffer allows dynamically enabling or disabling all clocks in the column level. The global clocks can drive RAM block clock inputs and reset, set, enable, and clock inputs to I/O registers. Furthermore, the quadrant clock outputs can be routed to all logic cell inputs.

Figure 13: PolarPro II Clock Network Architecture



Of the five global clock networks:

- Two can be either driven directly by clock pads, Configurable Clock Manager (CCM) outputs, or internally generated signals. These two global clocks go through 3-input global clock muxes located in the middle of the die. See **Figure 14** for a diagram of a 3-input global clock mux.
- Two can be either driven directly by clock pads or internally generated signals.
- One is a dedicated global clock network that goes directly to the quadrant clock network and is used as a dedicated fast clock.

Figure 14: Global Clock Structure

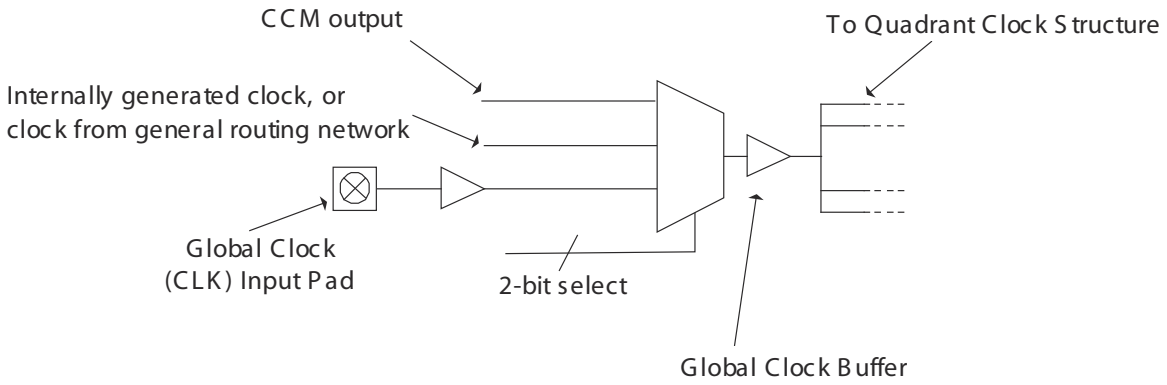
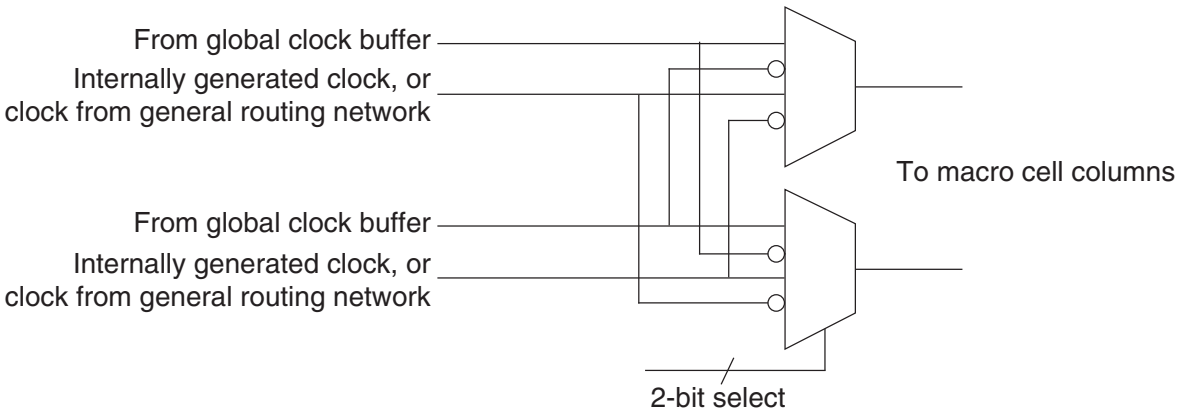


Figure 15 illustrates the quadrant HSCK 4-input mux.

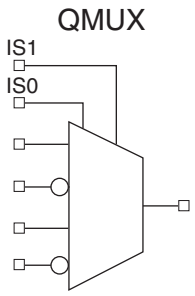
Figure 15: Quadrant Clock Structure



The quadrant HSCK mux is located at the middle of the quadrant. These 4-input HSCK muxes output inverted or non-inverted output from global HSCK, or inverted or non-inverted quad level HSCK depending on the 2-bit select line.

A quadrant HSCK mux can be implemented in Verilog, VHDL, and schematic designs by instantiating the quadrant HSCK mux macro, QMUX. **Figure 16** shows the schematic representation of the QMUX macro.

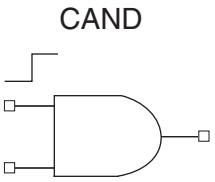
Figure 16: QMUX Macro



It is important to note that the select lines for the global clock and quadrant clock muxes are static signals and cannot be changed dynamically during device operation.

Using the column clock buffers, all clocks can be dynamically disabled at the column level. Column clock buffers can be implemented in Verilog, VHDL, and schematic designs by instantiating the column clock buffer macro, CAND. **Figure 17** shows the schematic representation of the CAND macro.

Figure 17: CAND Macro

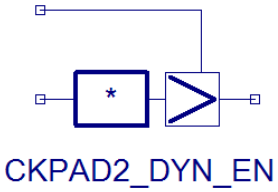


Dynamic Clock Enable

The QuickLogic PolarPro II QL2P150 devices provide a powerful dynamic clock enable feature that allows designers to dynamically enable and disable clocks routed into the QuickLogic device. Associated with each of the five clock inputs is a clock enable, which is an interface signal that can be either dynamically controlled via a routable signal or tied high or low. Once an incoming clock is disabled, the clock is driven low internally. All the logic that is driven by the clock is held at the state when the clock was disabled. If a reset signal is passed through the clock pad, the dynamic disable should not be used.

As an additional feature, PolarPro II devices have built-in deglitching circuitry to prevent clock glitching during transitions so that clocks can be enabled or disabled asynchronously without the possibility of false edge detection within the internal logic. The dynamic clock disable feature can be implemented in Verilog, VHDL, and schematic designs by instantiating the dynamic clock enable macro, CKPAD2_DYN_EN. **Figure 18** shows the schematic representation of the dynamic clock enable macro.

Figure 18: Clock Pad Macro for Dynamic Clock Enable

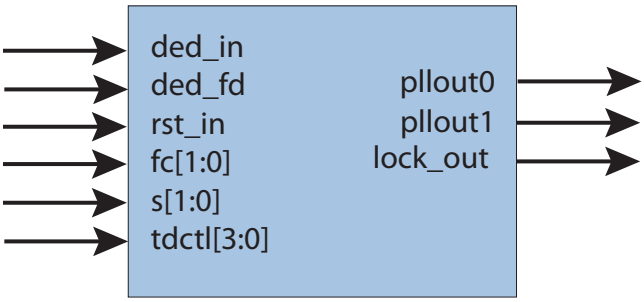


Configurable Clock Manager

The CCM features include:

- Input frequency range from 10 MHz to 150 MHz
- Output frequency range from 25 MHz to 200 MHz
- Output jitter is less than 200 ps peak-to-peak
- Two outputs: pullout0 (with 0° phase shift), and pullout1 (with an option of 0°, 90°, 180°, or 270° phase shift plus a programmable delay).
- Programmable delay allows delays up to 2.5 ns at 250 ps intervals (typical)
- Fixed feedback path
- Output frequency lock time in less than 10 µs

Figure 19: Configurable Clock Manager



The reset signal can be routed from a clock pad or generated using internal logic. The lock_out signal can be routed to internal logic and/or an output pad. CCM clock outputs can drive the global clock networks, as well as any general purpose I/O pin. Once the CCM has synchronized the output clock to the incoming clock, the lock_out signal will be asserted to indicate that the output clock is valid. Lock detection requires at least 10 µs after reset to assert lock_out. The PolarPro II CCMs have three modes of operation, based on the input frequency and desired output frequency. **Table 13** indicates the features of each mode.

Table 13: CCM PLL Mode Frequencies

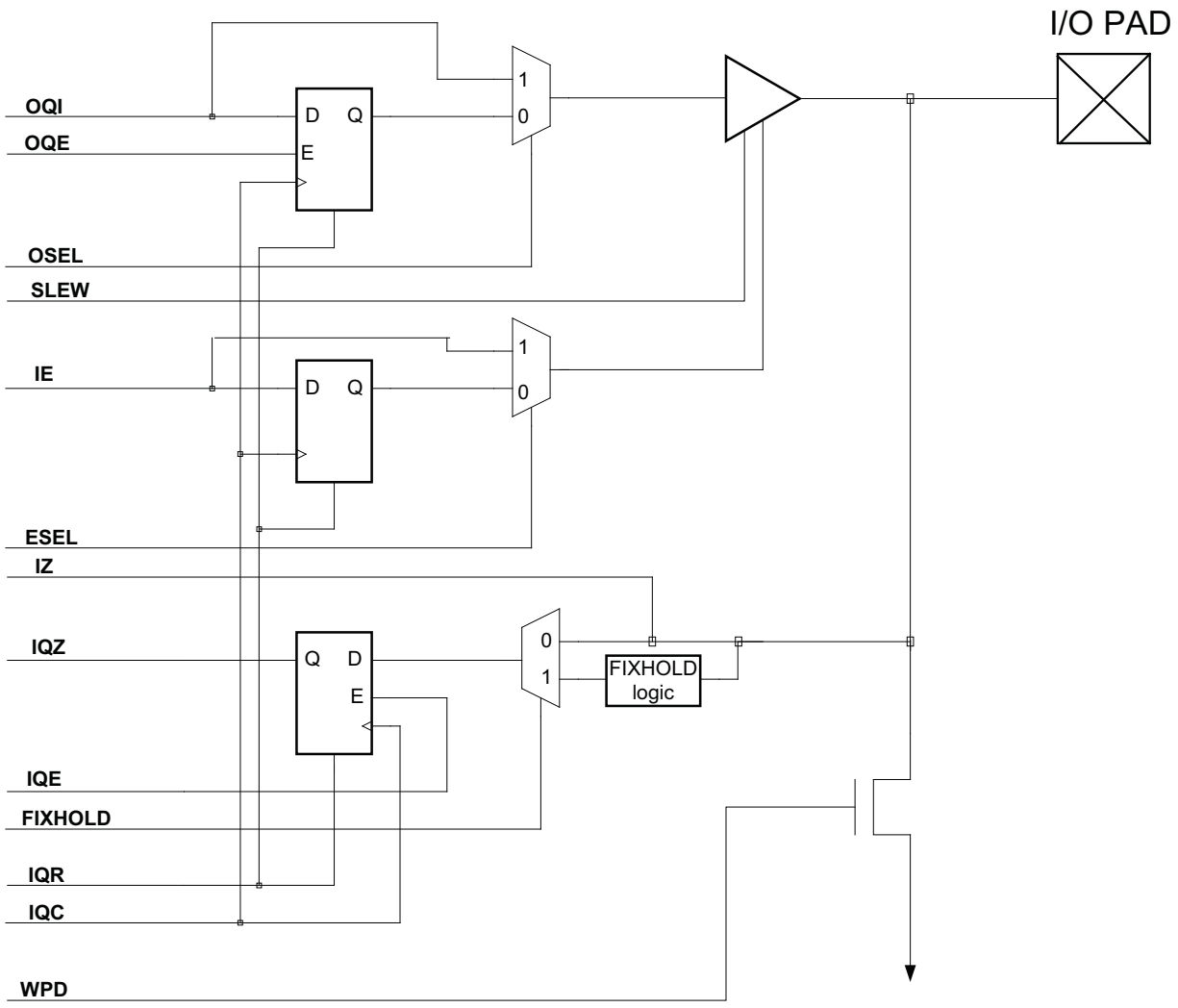
Output Frequency	Input Frequency Range	Output Frequency Range	PLL Mode
x1	25 MHz to 150 MHz	25 MHz to 150 MHz	PLL_MULT1
x2	15 MHz to 100 MHz	30 MHz to 200 MHz	PLL_MULT2
x4	10 MHz to 50 MHz	40 MHz to 200 MHz	PLL_MULT4

General Purpose Input Output (GPIO) Cell Structure

The GPIO features include:

- Direct or registered input with input path select
- Direct or registered output with output path select
- Direct or registered output enable with OE path select
- Input buffer enable to reduce power
- Programmable pull-down control
- Configurable slew rate
- Support for JTAG boundary scan

Figure 20: PolarPro II GPIO Cell



With bi-directional I/O pins and global clock input pins, the PolarPro II device maximizes I/O performance, functionality, and flexibility. All input and I/O pins are 1.8 V, 2.5 V, and 3.3 V tolerant and comply with the specific I/O standard selected. For single-ended I/O standards, the corresponding VCCIO bank input specifies the input tolerance and the output drive voltage. A weak pull-down function can be configured for an individual I/O. **Table 14** lists the GPIO interface signals.

Table 14: GPIO Interface Signals

Signal Name	Direction	Function
Routable Signals		
OQI	I	Output path input
OQE	I	Output register enable signal
IE	I	Enable path input
IZ	O	Input path combinatorial output to routing
IQZ	O	Input path register output to routing
IQE	I	Input register enable signal
IQC	I	Register clock
IQR	I	Register reset
PAD	I/O	I/O pad
Static Signals		
ESEL	I	Enable register/combinatorial path select '1' : combinatorial '0' : register
OSEL	I	Output register/combinatorial path select '1' : combinatorial '0' : register
SLEW	I	SLEW selection '0' : Slow slew '1' : Fast slew
FIX_HOLD	I	Input delay path selection '0' : Non-delay '1' : Delayed
WPD	I	Weak pull-down '0' : Disable - no weak pull-down '1' : Enable - weak pull-down enabled

Programmable Pull-Down

PolarPro II I/O supports Weak Pull-Down. A programmable Weak Pull-Down resistor is available on each I/O. The I/O Weak Pull-Down eliminates the need for external pull-down resistors. When WPD = 1, Weak Pull-Down is enabled.

Programmable Slew Rate

Each I/O has programmable slew rate capability. The PolarPro II GPIOs allow up to two different slew rate speeds (slow and fast). Slow slew rates can be used to reduce noise caused by I/O switching.

I/O interface standards are programmable on a per bank basis. **Table 15** illustrates the I/O bank configurations available. Each I/O bank is independent of other I/O banks and each I/O bank has its own VCCIO supply inputs. A mixture of different I/O standards can be used on a PolarPro II device. However, there is a limitation as to which I/O standards can be supported within a given bank. Only standards that share a common VCCIO can be shared within the same bank (e.g., PCI and LVTTL).

Table 15: I/O Standards and Applications

I/O Standard	VCCIO Voltage	Application
LVTTL	3.3 V	General Purpose
LVCMOS25	2.5 V	General Purpose
LVCMOS18	1.8 V	General Purpose
PCI	3.3 V	PCI Bus Applications

Very Low Power (VLP) Mode

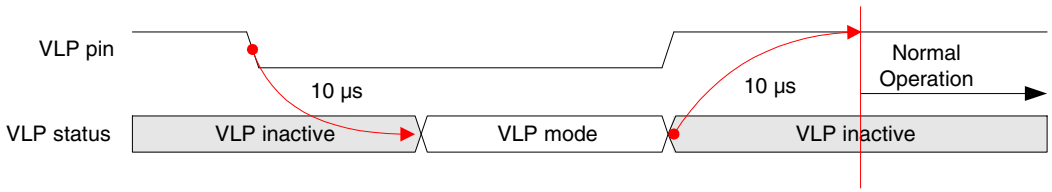
The QuickLogic PolarPro II devices have a unique feature, referred to as VLP mode, which reduces power consumption by placing the device in standby. Specifically, VLP mode can bring the total standby current down to less than 4.2 µA at room temperature when no incoming signals are toggled. The active low VLP pin controls VLP mode. For normal operation, the VLP pin must be driven to a voltage anywhere between 1.8 V and 3.3 V. If VLP is tied to 1.8 V, the VPUMP pin can be tied to 3.3 V for data retention in VLP mode, or to 0 V which does not allow data retention in VLP mode and draws additional current during normal operation. If VLP is tied to 1.5 V, the VPUMP pin must be tied to 3.3 V for VLP mode to be operational.

When the PolarPro II solution platform goes into VLP mode, the following occurs:

- All logic cell registers and GPIO registers values are held
- All RAM cell data is retained
- The outputs from all GPIO to the internal logic are tied to '0'
- GPIO outputs drive the previous values
- GPIO output enables retain the previous values
- Clock pad inputs are gated
- CCM is held in the reset state

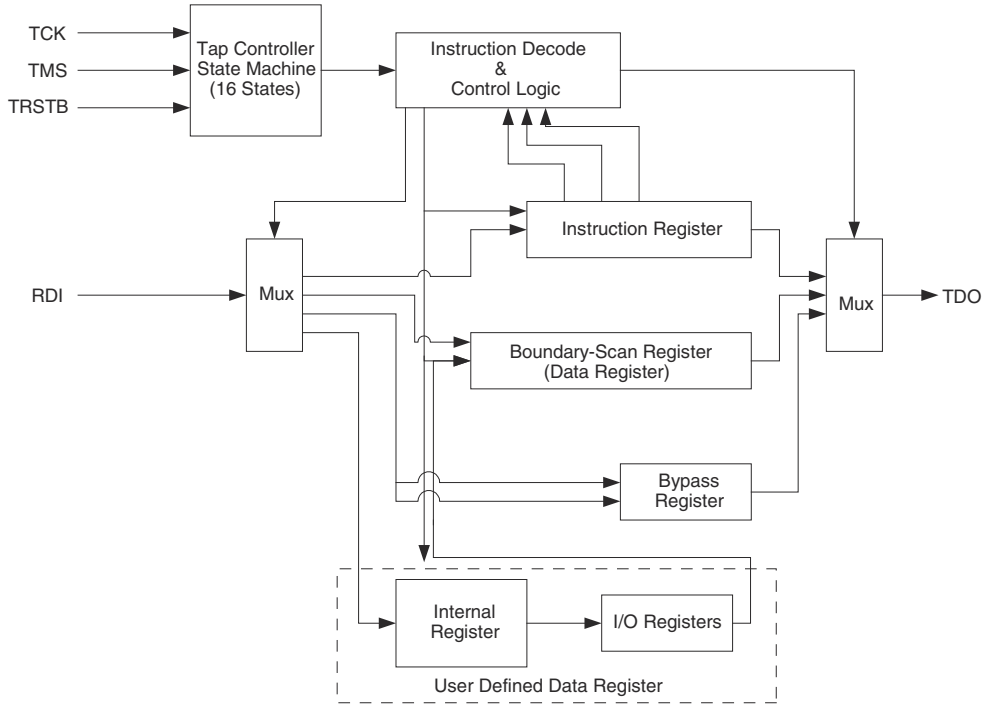
The entire operation from normal mode to VLP mode requires 10 µs. As the device exits out of VLP mode, which also takes 10 µs, the data from the registers, RAM, and GPIO are used to recover the functionality of the device. Furthermore, since the CCM was in a reset state during VLP mode, it must re-acquire the correct output signal before asserting lock_out. **Figure 21** displays the delays associated with entering and exiting VLP mode.

Figure 21: Typical VLP Mode Timing



Joint Test Access Group (JTAG) Information

Figure 22: JTAG Block Diagram



QuickLogic's PolarPro II devices comply with IEEE standard 1149.1, the Standard Test Access Port and Boundary Scan Architecture. The JTAG boundary scan test methodology allows complete observation and control of the boundary pins of a JTAG-compatible device through JTAG software. A Test Access Port (TAP) controller works in concert with the Instruction Register (IR), which allow users to run three required tests along with several user-defined tests. JTAG tests allow users to reduce system debug time, reuse test platforms and tools, and reuse subsystem tests for comprehensive verification of higher level system elements.

The 1149.1 standard requires the following three tests:

- **Extest Instruction.** The Extest Instruction performs a printed circuit board (PCB) interconnect test. This test places a device into an external boundary test mode, selecting the boundary scan register to be connected between the TAP Test Data In (TDI) and Test Data Out (TDO) pins. Boundary scan cells are preloaded with test patterns (through the Sample/Preload Instruction), and input boundary cells capture the input data for analysis.
- **Sample/Preload Instruction.** The Sample/Preload Instruction allows a device to remain in its functional mode, while selecting the boundary scan register to be connected between the TDI and TDO pins. For this test, the boundary scan register can be accessed through a data scan operation, allowing users to sample the functional data entering and leaving the device.
- **Bypass Instruction.** The Bypass Instruction allows data to skip a device boundary scan entirely, so the data passes through the bypass register. The Bypass instruction allows users to test a device without passing through other devices. The bypass register is connected between the TDI and TDO pins, allowing serial data to be transferred through a device without affecting the operation of the device.

JTAG Boundary Scan Description Language (BSDL) Support

- Machine-readable data for test equipment to generate testing vectors and software
- BSDL files available for all device/package combinations from QuickLogic
- Extensive industry support available and ATVG (Automatic Test Vector Generation)

Electrical Specifications

DC Characteristics

The DC Specifications are provided in **Table 16** through **Table 21**.

Table 16: Absolute Maximum Ratings

Parameter	Value	Parameter	Value
VCC Voltage	-0.5 V to 2.2 V	ESD Pad Protection	2 kV
VCCIO Voltage	-0.5 V to 4.0 V	Leaded Package Storage Temperature	-65° C to + 150° C
Input Voltage	-0.5 V to 4.0 V	Laminate Package (BGA) Storage Temperature	-55° C to + 125° C
Latch-up Immunity	±100 mA		

Table 17: Recommended Operating Range

Symbol	Parameter	Industrial		Commercial		Unit
		Min.	Max.	Min.	Max.	
VCC	Supply Voltage	1.43	1.89	1.43	1.89	V
VCCIO	I/O Input Tolerance Voltage	1.71	3.60	1.71	3.60	V
TJ	Junction Temperature	-40	100	0	85	°C

Table 18: DC Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
I_I	I or I/O Input Leakage Current	VI = VCCIO or GND	-1	-	1	µA
I_{OZ}	3-State Output Leakage Current	VI = VCCIO or GND	-	-	1	µA
C_I	I/O Input Capacitance	VCCIO = 3.6 V	-	-	8	pF
		VCCIO = 2.85 V	-	-	8	pF
C_{CLOCK}	Clock Input Capacitance	VCCIO = 3.6 V	-	-	8	pF
		VCCIO = 2.85 V	-	-	8	pF
I_{PD}	Current on Programmable Pull-Down @ VCC -= 1.8 V	VCCIO = 3.6 V	-	-	100	µA
		VCCIO = 2.85 V	-	-	100	µA
		VCCIO = 2.75 V	-	-	100	µA
		VCCIO = 1.89 V	-	-	100	µA
I_{VLP}	Quiescent Current on VLP Pin	VLP=3.3 V	-	0	5	µA
		VLP = 2.85 V	-	0	5	µA
I_{VPUMP}	Quiescent Current on VPUMP Pin	VPUMP=3.6 V	-	0	5	µA
		VPUMP = 2.85 V	-	0	5	µA
I_{CCM}	Quiescent Current on each CCMVCC	VCC=1.89 V	-	1	10	µA
		VCC = 1.50 V	-	1	10	µA
I_{VCCIO}	Quiescent Current on VCCIO	VCCIO = 3.6 V	-	2	10	µA
		VCCIO = 2.85	-	2	10	µA
		VCCIO = 2.75 V	-	2	10	µA
		VCCIO = 1.89 V	-	2	10	µA

NOTE: The process variation leakage can be up to 15% (at Vpump = 0 V) and 3% (at Vpump = 2.85 V)

Table 19: I_{VCC} Quiescent Current – 1.8 V

Conditions	-40°C (in µA)	0°C (in µA)	25°C (in µA)	70°C (in µA)	85°C (in µA)	100°C (in µA)
Vcc@1.71V, Vpump@2.57V, VLP@0V	0	2	3	17	27	45
Vcc@1.71V, Vpump@0V, VLP@2.57V	84	84	87	107	123	148
Vcc@1.71V, Vpump@2.57V, VLP@2.57V	4	8	13	38	49	78
Vcc@1.80V, Vpump@2.85V, VLP@0V	1	2	4	17	28	46
Vcc@1.80V, Vpump@0V, VLP@2.85V	100	101	104	127	145	172
Vcc@1.80V, Vpump@2.85V, VLP@2.85V	6	10	16	41	61	90
Vcc@1.89V, Vpump@3.14V, VLP@0V	1	2	4	18	29	48
Vcc@1.89V, Vpump@0V, VLP@3.14V	118	119	124	150	171	202
Vcc@1.89V, Vpump@3.14V, VLP@3.14V	7	13	20	48	73	105

NOTE: The process variation leakage can be up to 15% (at Vpump = 0 V) and 3% (at Vpump = 2.85 V)

Table 20: I_{VCC} Quiescent Current – 1.5 V

Conditions	-40°C (in µA)	0°C (in µA)	25°C (in µA)	70°C (in µA)	85°C (in µA)	100°C (in µA)
Vcc@1.43V, Vpump@2.79V, VLP@0V	0	1	3	14	24	38
Vcc@1.43V, Vpump@0V, VLP@2.57V	47	49	52	63	76	93
Vcc@1.43V, Vpump@2.79V, VLP@2.57V	2	4	7	22	34	52
Vcc@1.50V, Vpump@2.85V, VLP@0V	0	1	3	14	24	40
Vcc@1.50V, Vpump@0V, VLP@2.85V	52	56	59	72	84	104
Vcc@1.50V, Vpump@2.85V, VLP@2.85V	2	5	8	24	37	36
Vcc@1.58V, Vpump@2.91V, VLP@0V	1	1	3	15	25	41
Vcc@1.58V, Vpump@0V, VLP@3.14V	63	66	69	84	96	118
Vcc@1.50V, Vpump@2.91V, VLP@3.14V	3	6	9	28	41	62

Table 21: DC Input and Output Levels[a]

Symbol	INREF		V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V_{MIN}	V_{MAX}	V_{MIN}	V_{MAX}	V_{MIN}	V_{MAX}	V_{MAX}	V_{MIN}	mA	mA
LVTTL	n/a	n/a	-0.3	0.8	2.2	VCCIO + 0.3	0.4	2.4	2.0	-2.0
LVCMOS2	n/a	n/a	-0.3	0.7	1.7	VCCIO + 0.3	0.7	1.7	2.0	-2.0
LVCMOS18	n/a	n/a	-0.3	0.63	1.2	VCCIO + 0.3	0.7	1.7	2.0	-2.0
PCI	n/a	n/a	-0.3	0.3 x VCCIO	0.6 x V_{CCIO}	VCCIO + 0.5	0.1 x VCCIO	0.9 x VCCIO	1.5	-0.5

a. The data provided in **Table 21** represents the JEDEC and PCI specification. QuickLogic devices either meet or exceed these requirements.

Package Thermal Characteristics

The PolarPro II solution platform is available for Commercial (0°C to 85°C Junction), Industrial (-40°C to 100°C Junction), and Military (-55°C to 125°C Junction) temperature ranges.

Thermal Resistance Equations:

$\theta_{JC} = (T_J - T_C)/P$
$\theta_{JA} = (TJ - TA)/P$
$P_{MAX} = (T_{JMAX} - T_{AMAX})/\theta_{JA}$

Parameter Description:

θ_{JC}: Junction-to-case thermal resistance

θ_{JA}: Junction-to-ambient thermal resistance

T_J: Junction temperature

T_A: Ambient temperature

P: Power dissipated by the device while operating

P_{MAX}: The maximum power dissipation for the device

T_{JMAX}: Maximum junction temperature

T_{AMAX}: Maximum ambient temperature

NOTE: Maximum junction temperature (T_{JMAX}) is 125°C. To calculate the maximum power dissipation for a device package look up θ_{JA} from **Table 22**, pick an appropriate T_{AMAX} and use: $P_{MAX} = (125°C - T_{AMAX})/ \theta_{JA.}$

Table 22: Package Thermal Characteristics

Package Description				Theta-JA (° C/W)
Device	Package Code	Package Type	Pin Count	0 LFM
QL2P150	PD	VFBGA (5 mm x 5 mm)	144	50.0
	PU	TFBGA (6 mm x 6 mm)	121	51.8
	WD	WLCSP (3.25 mm x 3.49 mm)	64	53.0

Power Consumption

Programmable Fabric Power Consumption

QuickLogic's ultra low power programmable fabric is ideal for implementing connectivity solutions, custom logic and processor interface. The standby current of the smallest PolarPro II solution platform fabric in VLP mode is as low as 4.2 µA. The dynamic power consumption varies depending on the operating conditions and what functions are used in the fabric. Contact your QuickLogic Customer Solution Architect (CSA) for specifics related to your use case.

Moisture Sensitivity Level

Table 23 describes the solder composition characteristics.

Table 23: Solder Composition

Package Type	Pin Count	Lead Type	Pb-Free	Moisture Sensitivity Level
VFBGA (5 mm x 5 mm)	144	BGA Solder	Sn-Ag-Cu	3
TFBGA (6 mm x 6 mm)	121	BGA Solder	Sn-3Ag-Cu (Sn4, Ag, Cu[a])	3
WLCSP (3.25 mm x 3.49 mm)	64	BGA Solder	Sn-1.0Ag-0.5Cu (Sn98.5, Ag1,Cu0.5)	1

a. Sn-3Ag-Cu (Sn, 4Ag, Cu) means that Ag can range from 3% to 4%. Cu is always 0.5%.

Reflow Profile

QuickLogic follows JEDEC specification JESD97 for lead-free devices. **Figure 23** shows the Pb-free component preconditioning reflow profile.

Figure 23: Pb-Free Component Preconditioning Reflow Profile

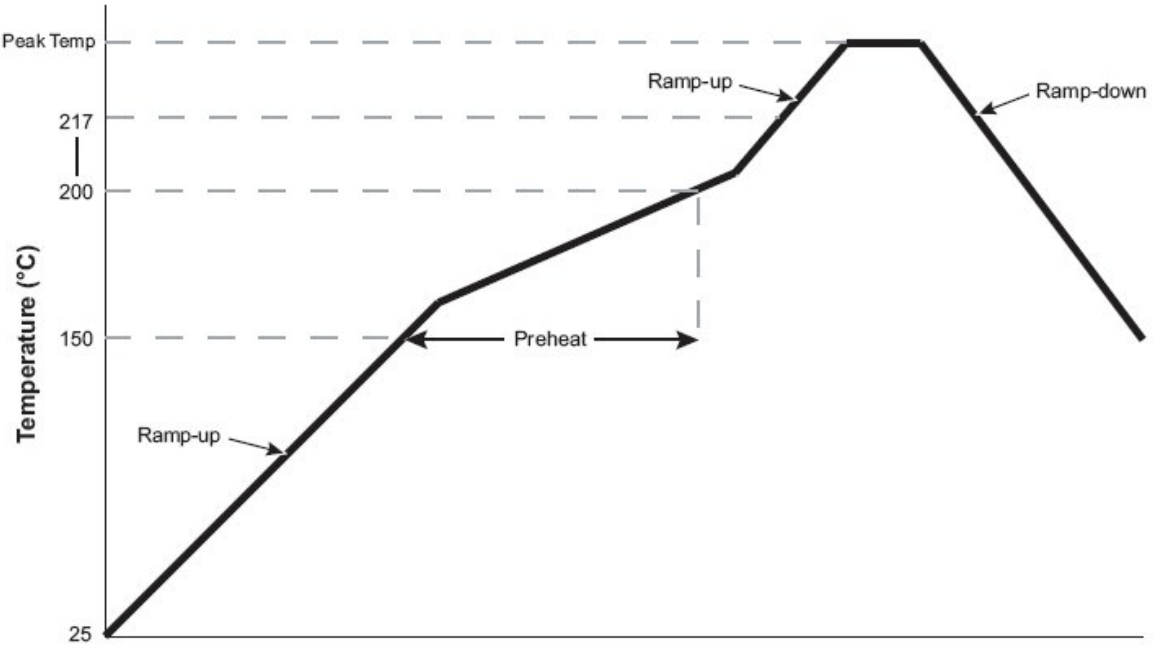


Table 24 shows the Pb-free component preconditioning reflow profile.

Table 24: Pb-Free Component Preconditioning Reflow Profile[a,b]

Profile Feature	Profile Conditions
Ramp-up rate	3°C/sec. max. (2°C/sec. typical)
Preheat time (from 150°C to 200°C)	60 to 120 sec. (80 to 100 sec. typical)
Time maintained above 217°C	60 to 150 sec. (80 to 100 sec. typical)
Peak temperature	260°C
Time within 5°C of actual peak	30 sec. max. (23 to 29 sec. typical)
Ramp-down rate	6°C/sec. max. (3°C/sec. typical)
Time from 25°C to peak temperature	8 min. max. (6 min. typical)

a. The above conditions are used for component qualifications. This should not be interpreted as the recommended profile for board mounting. Customers should optimize their board mounting reflow profile based on their specific conditions such as board design, solder paste, etc.
b. All temperatures are measured on the package body surface.

Power-Up Sequencing

Figure 24: Power-Up Sequencing

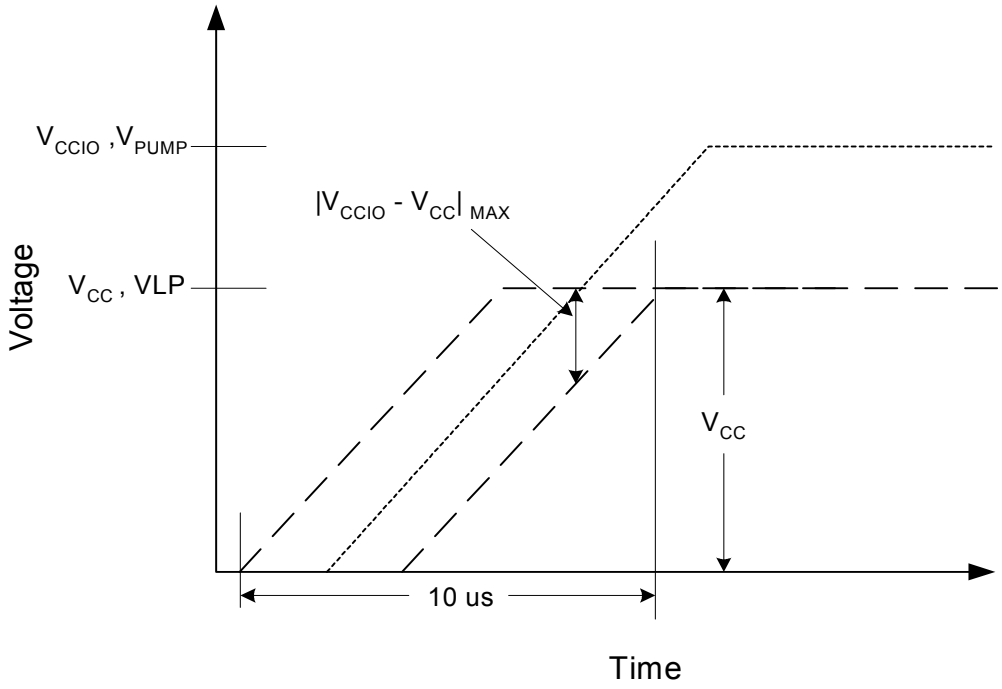


Figure 24 shows an example where all VCCIO = 3.3 V, VPUMP = 3.3 V and VLP = 1.8 V. When powering up a PolarPro II solution platform, VCC, VCCIO rails must take 10 µs or longer to reach the maximum value (refer to **Figure 24**). Ramping VCC and VCCIO faster than 10 µs can cause the device to behave improperly.

It is also important to ensure VCCIO and VLP are within 500 mV of VCC when ramping up the power supplies. In the case where VCCIO or VLP are greater than VCC by more than 500 mV an additional current draw can occur as VCC passes its threshold voltage. In a case where VCC is greater than VCCIO by more than 500 mV the protection diodes between the power supplies become forward biased. If this occurs then there will be an additional current load on the power supply. Having the diodes on can cause a reliability problem, since it can wear out the diodes and subsequently damage the internal transistors.

Programming Stipulation

For PolarPro II devices to correctly program, there must not be any race conditions or internally generated free-running oscillators in the design. This will cause an ICC programming failure during the programming process. QuickLogic cannot guarantee the operation of any device that fails programming. Therefore, race conditions and free-running oscillators must be removed from designs so that PolarPro II devices can correctly pass programming.

Pin Descriptions

Table 25: Pin Descriptions

Pin	Direction	Function	Description
Dedicated Pin Descriptions			
GPIO(H:A)	I/O	General purpose input/output pin	The I/O pin is a bi-directional pin, configurable to either an input-only, output-only, or bi-directional pin. The letter inside the parenthesis means that the I/O is located in the bank with that letter. If an I/O is not used, the development software provides the option of tying that pin to GND, VCCIO, or Hi-Z.
CLK(H:G) CLK(D:C)	I	Global clock network pin low skew global clock	This pin provides access to a distributed network capable of driving the CLOCK, SET, RESET, all inputs to the logic cell, Read and Write clocks, Read and Write enables of the embedded RAM blocks, and I/O inputs. Additionally, the clock networks can be accessed from internal routing. Meaning, clock signals do not necessarily need to come into the device from a clock pin.
DEDCLK(H)	I	Dedicated clock network pin low skew clock	This pin provides access to a distributed network capable of driving the CLOCK, SET, RESET, all inputs to the logic cell, Read and Write clocks, Read and Write enables of the embedded RAM blocks, and I/O inputs. The voltage tolerance of this pin is specified by VCCIO.
CCMIN(H)	I	CCM clock input	Input clock for CCM. The voltage tolerance for this pin is specified by VCCIO(H).
CCMVCC	I	Power supply pin for CCM	CCM input voltage level. Configurable as 1.8 V only.
CCMGND	I	Ground pin for CCM	Connect to ground.
VLP	I	Voltage low power	Active low. Therefore, when VLP is 0 V, the device will go into low power mode. For the WLCSP package, tie VLP to 1.8 V. For lowest possible power, VCCIO(D) must be a 1.8 V bank. For the VFBGA package, tie VLP to 1.8 V or VCCIO(D).
VPUMP	I	Charge Pump Disable	VPUMP = 0 V or 3.3 V. If VPUMP = 0 V, refer to **Table 19** on page 28 and **Table 20** on page 28 for power consumption information.
VCC	I	Power supply pin	Connect to 1.8 V or 1.5 V supply. When VCC is 1.5 V, timing will be about 35% slower.
VCCIO(H:A)	I	Input voltage tolerance pin	This pin provides the flexibility to interface the device with either a 3.3 V, 2.5 V, or 1.8 V device. The letter inside the parenthesis means that the VCCIO is located in the bank with that letter. Every I/O pin in the same bank will be tolerant of the same VCCIO input signals and will drive VCCIO level output signals. Even if certain VCCIO banks are not used, all VCCIO pins must be driven when the device is powered up. For the WLCSP package, use VCCIO(D) at 1.8 V for the lowest possible static power.

Table 25: Pin Descriptions *(Continued)*

Pin	Direction	Function	Description
GND	I	Ground pin	Connect to ground.
JTAG Pin Descriptions			
TDI	I	Test data in for JTAG	The I/O standard for this pin is specified by VCCIO(D). Connect to GND if unused.
TRSTB	I	Active low reset for JTAG	The I/O standard for this pin is specified by VCCIO(D). Connect to GND if unused.
TMS	I	Test mode select for JTAG	The I/O standard for this pin is specified by VCCIO(D). Connect to GND if unused.
TCK	I	Test clock for JTAG	The I/O standard for this pin is specified by VCCIO(D). Connect to GND if unused.
TDO	O	Test data out for JTAG	The output level drive is specified by VCCIO(D). Must be left unconnected if not used for JTAG.

Recommended Unused Pin Terminations for PolarPro II Devices

All unused, general purpose I/O pins can be tied to VCCIO, GND, or Hi-Z (high impedance) internally. By default, QuickLogic QuickWorks software ties unused I/Os to GND.

Terminate the rest of the pins at the board level as recommended in **Table 26**.

Table 26: Recommended Unused Pin Terminations

Signal Name	Recommended Termination
CLK <x>[a]	Connect to GND or VCCIO(x) if unused.
VLP	For the WLCSP package, tie VLP to 1.8 V. For lowest possible power, VCCIO(D) must be a 1.8 V bank. For the VFBGA package, tie VLP to 1.8 V or VCCIO(D).
CCMVCC	If a CCM is not used, the corresponding CCMVCC must be tied to 1.8V. When a CCM is not used, the software tools will automatically configure the device to hold the CCM in a reset state.
TDI	Connect to GND if not used for JTAG.
TRSTB	Connect to GND if not used for JTAG.
TMS	Connect to GND if not used for JTAG.
TCK	Connect to GND if not used for JTAG.
TDO	Must be left unconnected if not used for JTAG.

a. x represents A, B, C, D, E, F, G, or H.

Packaging Pinout Tables

PolarPro II QL2P150 – 64-Ball (3.25 mm x 3.49 mm) WLCSP Pinout Table

Table 27: PolarPro II QL2P150 – 64-Ball (3.25 mm x 3.49 mm) WLCSP Pinout Table

Ball	Function	Ball	Function	Ball	Function	Ball	Function
A1	VCC	C1	VCC	E1	VCCIO(D)	G1	GPIO(C)
A2	GPIO(H)	C2	GPIO(H)	E2	GPIO(C)	G2	GPIO(C)
A3	CCMIN(H)/CLK(H)/ GPIO(H)	C3	GPIO(H)	E3	GPIO(C)	G3	GPIO(C)
A4	DEDCLK(H)/GPIO(H)	C4	VCC	E4	VCCIO(C)	G4	GPIO(C)
A5	CLK(G)/GPIO(G)	C5	GPIO(G)	E5	GPIO(C)	G5	GPIO(D)
A6	GPIO(G)	C6	GPIO(G)	E6	VCCIO(D)	G6	GPIO(D)
A7	GPIO(G)	C7	GPIO(G)	E7	GPIO(D)	G7	GPIO(D)
A8	GPIO(G)	C8	VCC	E8	VCCIO(D)	G8	GPIO(D)
B1	VCC	D1	VCC	F1	GPIO(C)	H1	GPIO(C)
B2	GPIO(H)	D2	VCCIO(H)	F2	GND	H2	VPUMP
B3	GPIO(H)	D3	GND	F3	GPIO(C)	H3	GPIO(C)
B4	GPIO(H)	D4	GND	F4	GPIO(C)	H4	GPIO(C)
B5	GPIO(G)	D5	GND	F5	GPIO(C)	H5	CLK(C)/GPIO(C)
B6	GPIO(G)	D6	GND	F6	GPIO(D)	H6	CLK(D)/GPIO(D)
B7	VCC	D7	VCCIO(G)	F7	GPIO(D)	H7	GPIO(D)
B8	VLP	D8	VCC	F8	VCCIO(E)[a]	H8	GND

a. Must tie to VCC or VCCIO.

PolarPro II QL2P150 – 121-Ball (6 mm x 6 mm) TFBGA Pinout Table

Table 28: PolarPro II QL2P150 – 121-Ball (6 mm x 6 mm) TFBGA Pinout Table

Ball	Function	Ball	Function	Ball	Function	Ball	Function
A1	VCC	C10	GPIO(H)	F8	VCC	J6	GND
A2	GPIO(G)	C11	GPIO(A)	F9	GPIO(A)	J7	GPIO(C)
A3	GPIO(G)	D1	GPIO(F)	F10	GPIO(A)	J8	GPIO(C)
A4	GPIO(G)	D2	GPIO(F)	F11	GPIO(A)	J9	GPIO(B)
A5	CLK(G)/GPIO(G)	D3	GPIO(F)	G1	TCK	J10	GPIO(B)
A6	DEDCLK(H)/GPIO(H)	D4	VCCIO(G)	G2	VCCIO(D)	J11	GPIO(B)
A7	GPIO(H)	D5	VCC	G3	GPIO(D)	K1	GND
A8	CCMIN(H)/CLK(H)/GPIO(H)	D6	GPIO(F)	G4	VCC	K2	GPIO(E)
A9	GPIO(H)	D7	GPIO(A)	G5	VCCIO(F)	K3	GPIO(D)
A10	GPIO(H)	D8	GPIO(C)	G6	GND	K4	GPIO(D)
A11	VCC	D9	GPIO(H)	G7	GND	K5	TDI
B1	VLP	D10	GPIO(A)	G8	VCC	K6	GPIO(D)
B2	GPIO(G)	D11	GPIO(A)	G9	TRSTB	K7	GPIO(C)
B3	GPIO(G)	E1	GPIO(F)	G10	GPIO(B)	K8	GPIO(C)
B4	GPIO(G)	E2	GPIO(F)	G11	GPIO(B)	K9	GPIO(C)
B5	GPIO(G)	E3	GPIO(F)	H1	GPIO(E)	K10	GPIO(B)
B6	TMS	E4	GPIO(F)	H2	GPIO(E)	K11	GPIO(B)
B7	GPIO(H)	E5	VCCIO(H)	H3	GPIO(E)	L1	VCC
B8	GPIO(H)	E6	GND	H4	GPIO(E)	L2	GPIO(D)
B9	GPIO(H)	E7	GND	H5	VCCIO(E)	L3	GPIO(D)
B10	CCMGND	E8	VCCIO(A)	H6	GND	L4	TDO
B11	GND	E9	VCCIO(B)	H7	VCCIO(D)	L5	CLK(C)/GPIO(C)
C1	GPIO(F)	E10	GPIO(A)	H8	VCCIO(C)	L6	CLK(D)/GPIO(D)
C2	GPIO(G)	E11	GPIO(A)	H9	VCCIO(D)	L7	GPIO(C)
C3	GPIO(G)	F1	GPIO(E)	H10	GPIO(B)	L8	GPIO(C)
C4	GPIO(G)	F2	GPIO(F)	H11	GPIO(B)	L9	VPUMP
C5	GPIO(G)	F3	GPIO(F)	J1	GPIO(E)	L10	GND
C6	GPIO(H)	F4	GND	J2	GPIO(E)	L11	VCC
C7	GPIO(H)	F5	GND	J3	GPIO(E)		
C8	GPIO(A)	F6	GND	J4	GPIO(D)		
C9	CCMVCC	F7	GND	J5	GPIO(D)		

PolarPro II QL2P150 – 144-Ball (5 mm x 5 mm) VFBGA Pinout Table

Table 29: PolarPro II QL2P150 – 144-Ball (5 mm x 5 mm) VFBGA Pinout Table

Ball	Function	Ball	Function	Ball	Function	Ball	Function
A1	GPIO(G)	D1	GPIO(F)	G1	VCCIO(D)	K1	GPIO(D)
A2	GPIO(G)	D2	GPIO(F)	G2	GPIO(E)	K2	GND
A3	GPIO(G)	D3	GPIO(F)	G3	GPIO(E)	K3	GPIO(D)
A4	GPIO(G)	D4	GPIO(G)	G4	GPIO(E)	K4	GPIO(D)
A5	GPIO(G)	D5	GPIO(G)	G5	GND	K5	GPIO(D)
A6	GPIO(H)	D6	GPIO(H)	G6	VCC	K6	TDI
A7	GPIO(H)	D7	GPIO(H)	G7	GND	K7	CLK(C)/GPIO(C)
A8	CCMIN(H)/CLK(H)/GPIO(H)	D8	VCCIO(H)	G8	VCC	K8	GPIO(C)
A9	GPIO(H)	D9	GPIO(H)	G9	GND	K9	GPIO(C)
A10	GPIO(H)	D10	VCC	G10	GPIO(B)	K10	GPIO(B)
A11	GPIO(H)	D11	GPIO(A)	G11	GPIO(B)	K11	GPIO(C)
A12	GPIO(H)	D12	GPIO(A)	G12	VCCIO(D)	K12	GPIO(B)
B1	VCCIO(G)	E1	GPIO(F)	H1	VCCIO(E)	L1	GPIO(D)
B2	GPIO(G)	E2	VCCIO(F)	H2	GPIO(E)	L2	GPIO(D)
B3	GPIO(G)	E3	GPIO(F)	H3	GPIO(E)	L3	GPIO(D)
B4	GPIO(G)	E4	GPIO(F)	H4	VCCIO(D)	L4	GPIO(D)
B5	GPIO(G)	E5	GPIO(G)	H5	GND	L5	GPIO(D)
B6	DEDCLK(H)/GPIO(H)	E6	GPIO(G)	H6	GND	L6	GPIO(D)
B7	TMS	E7	GPIO(H)	H7	VCC	L7	GPIO(C)
B8	GPIO(H)	E8	VCC	H8	GND	L8	VCCIO(C)
B9	GPIO(H)	E9	GND	H9	GPIO(C)	L9	GPIO(C)
B10	GPIO(H)	E10	GPIO(A)	H10	GPIO(B)	L10	VPUMP
B11	CCMGND	E11	VCCIO(A)	H11	GPIO(B)	L11	GPIO(C)
B12	GND	E12	GPIO(A)	H12	GPIO(B)	L12	GPIO(C)
C1	VLP	F1	GPIO(F)	J1	GPIO(E)	M1	GND
C2	GPIO(G)	F2	GPIO(F)	J2	GPIO(E)	M2	GPIO(D)
C3	GPIO(G)	F3	GPIO(F)	J3	GPIO(E)	M3	GPIO(D)
C4	GPIO(G)	F4	TCK	J4	TDO	M4	GPIO(D)
C5	GPIO(G)	F5	GND	J5	GND	M5	GPIO(D)
C6	CLK(G)/GPIO(G)	F6	VCC	J6	GPIO(D)	M6	CLK(D)/GPIO(D)
C7	GPIO(H)	F7	VCC	J7	GPIO(C)	M7	GPIO(C)
C8	GPIO(H)	F8	GND	J8	GPIO(C)	M8	GPIO(C)
C9	GPIO(H)	F9	VCC	J9	GPIO(C)	M9	GPIO(C)
C10	GPIO(A)	F10	GPIO(A)	J10	GPIO(B)	M10	GPIO(C)
C11	GPIO(A)	F11	TRSTB	J11	VCCIO(B)	M11	GPIO(C)
C12	CCMVCC	F12	GPIO(A)	J12	GPIO(B)	M12	GND

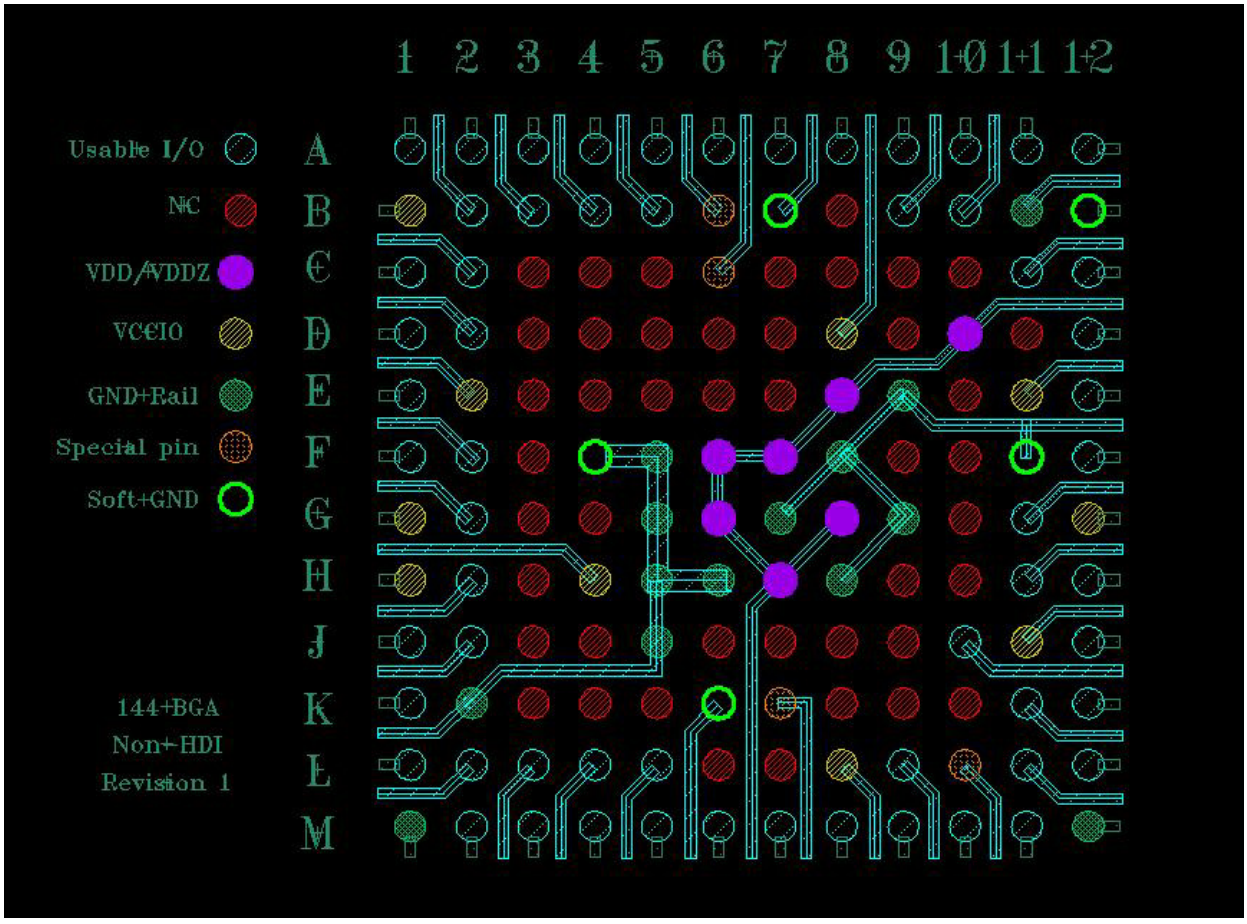
Non-HDI PolarPro II QL2P150 – 144-Ball (5 mm x 5 mm) VFBGA Pinout Table

Table 30: Non-HDI PolarPro II QL2P150 – 144-Ball (5 mm x 5 mm) VFBGA Pinout Table

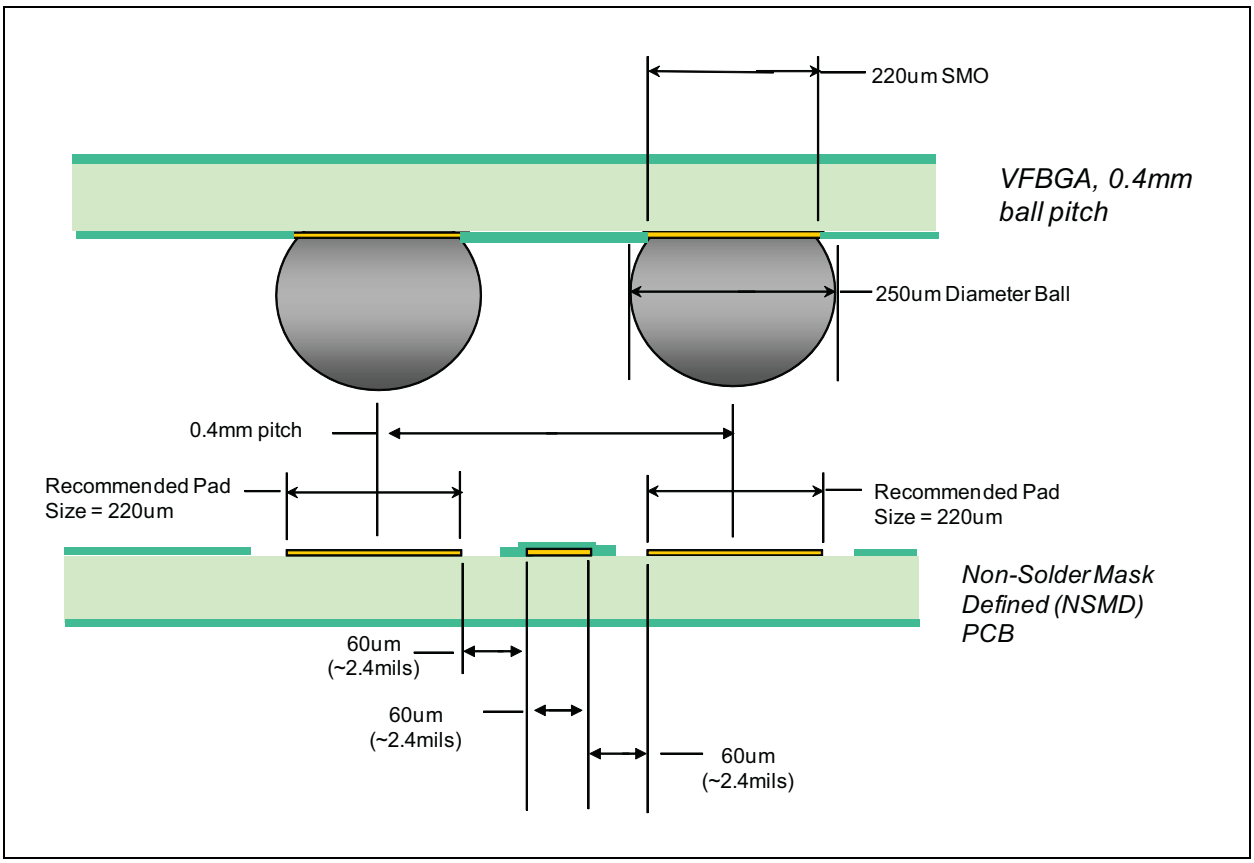
Ball	Function	Non-HDI	Ball	Function	Non-HDI	Ball	Function	Non-HDI	Ball	Function	Non-HDI
A1	GPIO(G)	Yes	D1	GPIO(F)	Yes	G1	VCCIO(D)	Yes	K1	GPIO(D)	Yes
A2	GPIO(G)	Yes	D2	GPIO(F)	Yes	G2	GPIO(E)	Yes	K2	GND	GND
A3	GPIO(G)	Yes	D3	GPIO(F)	Float	G3	GPIO(E)	Float	K3	GPIO(D)	Float
A4	GPIO(G)	Yes	D4	GPIO(G)	Float	G4	GPIO(E)	Float	K4	GPIO(D)	Float
A5	GPIO(G)	Yes	D5	GPIO(G)	Float	G5	GND	GND	K5	GPIO(D)	Float
A6	GPIO(H)	Yes	D6	GPIO(H)	Float	G6	VCC	VCC	K6	TDI	Yes
A7	GPIO(H)	Yes	D7	GPIO(H)	Float	G7	GND	GND	K7	CLK(C)/GPIO(C)	Yes
A8	CCMIN(H)/ CLK(H)/GPIO(H)	Yes	D8	VCCIO(H)	Yes	G8	VCC	VCC	K8	GPIO(C)	Float
A9	GPIO(H)	Yes	D9	GPIO(H)	Float	G9	GND	GND	K9	GPIO(C)	Float
A10	GPIO(H)	Yes	D10	VCC	VCC	G10	GPIO(B)	Float	K10	GPIO(B)	Float
A11	GPIO(H)	Yes	D11	GPIO(A)	Float	G11	GPIO(B)	Yes	K11	GPIO(C)	Yes
A12	GPIO(H)	Yes	D12	GPIO(A)	Yes	G12	VCCIO(D)	Yes	K12	GPIO(B)	Yes
B1	VCCIO(G)	Yes	E1	GPIO(F)	Yes	H1	VCCIO(E)	Yes	L1	GPIO(D)	Yes
B2	GPIO(G)	Yes	E2	VCCIO(F)	Yes	H2	GPIO(E)	Yes	L2	GPIO(D)	Yes
B3	GPIO(G)	Yes	E3	GPIO(F)	Float	H3	GPIO(E)	Float	L3	GPIO(D)	Yes
B4	GPIO(G)	Yes	E4	GPIO(F)	Float	H4	VCCIO(D)	Yes	L4	GPIO(D)	Yes
B5	GPIO(G)	Yes	E5	GPIO(G)	Float	H5	GND	GND	L5	GPIO(D)	Yes
B6	DEDCLK(H)/ GPIO(H)	Yes	E6	GPIO(G)	Float	H6	GND	GND	L6	GPIO(D)	Float
B7	TMS	Yes	E7	GPIO(H)	Float	H7	VCC	VCC	L7	GPIO(C)	Float
B8	GPIO(H)	Float	E8	VCC	VCC	H8	GND	GND	L8	VCCIO(C)	Yes
B9	GPIO(H)	Yes	E9	GND	GND	H9	GPIO(C)	Float	L9	GPIO(C)	Yes
B10	GPIO(H)	Yes	E10	GPIO(A)	Float	H10	GPIO(B)	Float	L10	VPUMP	Yes
B11	CCMGND	Yes	E11	VCCIO(A)	Yes	H11	GPIO(B)	Yes	L11	GPIO(C)	Yes
B12	GND	Yes	E12	GPIO(A)	Yes	H12	GPIO(B)	Yes	L12	GPIO(C)	Yes
C1	VLP	Yes	F1	GPIO(F)	Yes	J1	GPIO(E)	Yes	M1	GND	Yes
C2	GPIO(G)	Yes	F2	GPIO(F)	Yes	J2	GPIO(E)	Yes	M2	GPIO(D)	Yes
C3	GPIO(G)	Float	F3	GPIO(F)	Float	J3	GPIO(E)	Float	M3	GPIO(D)	Yes
C4	GPIO(G)	Float	F4	TCK	GND	J4	TDO	Float	M4	GPIO(D)	Yes
C5	GPIO(G)	Float	F5	GND	GND	J5	GND	GND	M5	GPIO(D)	Yes
C6	CLK(G)/GPIO(G)	Yes	F6	VCC	VCC	J6	GPIO(D)	Float	M6	CLK(D)/GPIO(D)	Yes
C7	GPIO(H)	Float	F7	VCC	VCC	J7	GPIO(C)	Float	M7	GPIO(C)	Yes
C8	GPIO(H)	Float	F8	GND	GND	J8	GPIO(C)	Float	M8	GPIO(C)	Yes
C9	GPIO(H)	Float	F9	VCC	VCC	J9	GPIO(C)	Float	M9	GPIO(C)	Yes
C10	GPIO(A)	Float	F10	GPIO(A)	Float	J10	GPIO(B)	Yes	M10	GPIO(C)	Yes
C11	GPIO(A)	Yes	F11	TRSTB	GND	J11	VCCIO(B)	Yes	M11	GPIO(C)	Yes
C12	CCMVCC	Yes	F12	GPIO(A)	Yes	J12	GPIO(B)	Yes	M12	GND	Yes

NOTE: See **Non-HDI PolarPro II QL2P150 – 144-Ball (5 mm x 5 mm) VFBGA PCB Routing View** on page 39. and **PolarPro II QL2P150 – 144-Ball (5 mm x 5 mm) VFBGA Typical PCB Land and Trace Width View** on page 40.

Non-HDI PolarPro II QL2P150 – 144-Ball (5 mm x 5 mm) VFBGA PCB Routing View



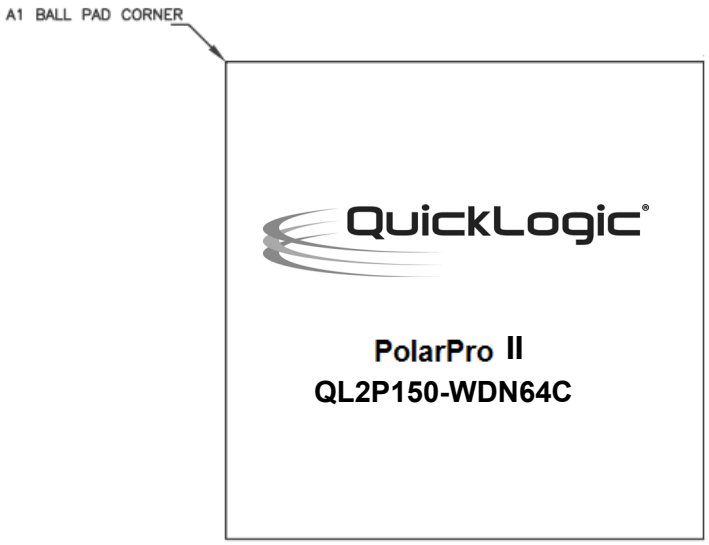
PolarPro II QL2P150 – 144-Ball (5 mm x 5 mm) VFBGA
Typical PCB Land and Trace Width View



Pinout Diagrams

PolarPro II QL2P150 – 64-Ball (3.25 mm x 3.49 mm) WLCSP

Top



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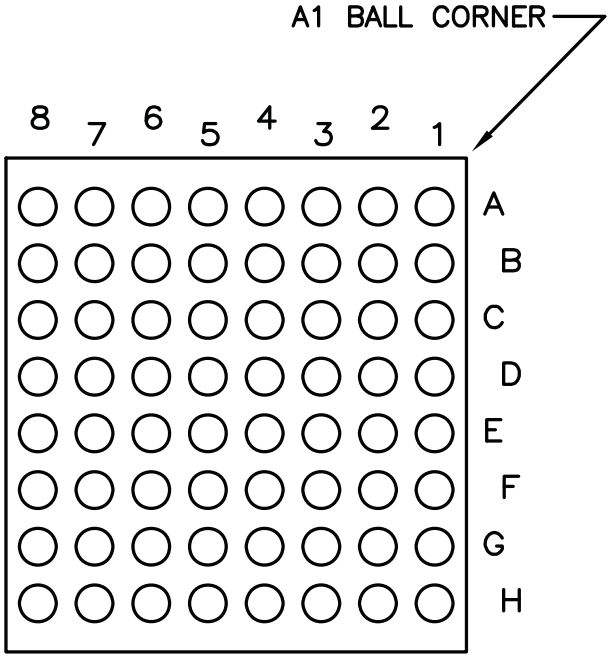
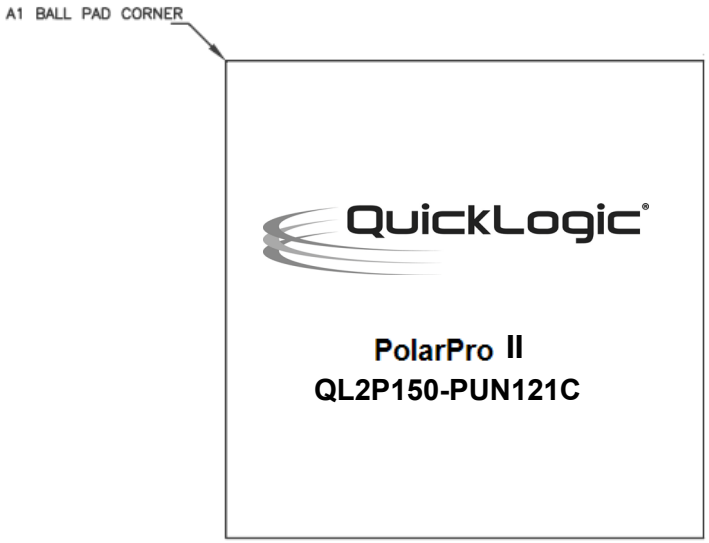


PolarPro II QL2P150 – 121-Ball (6 mm x 6 mm) TFBGA Pinout Diagram

Top



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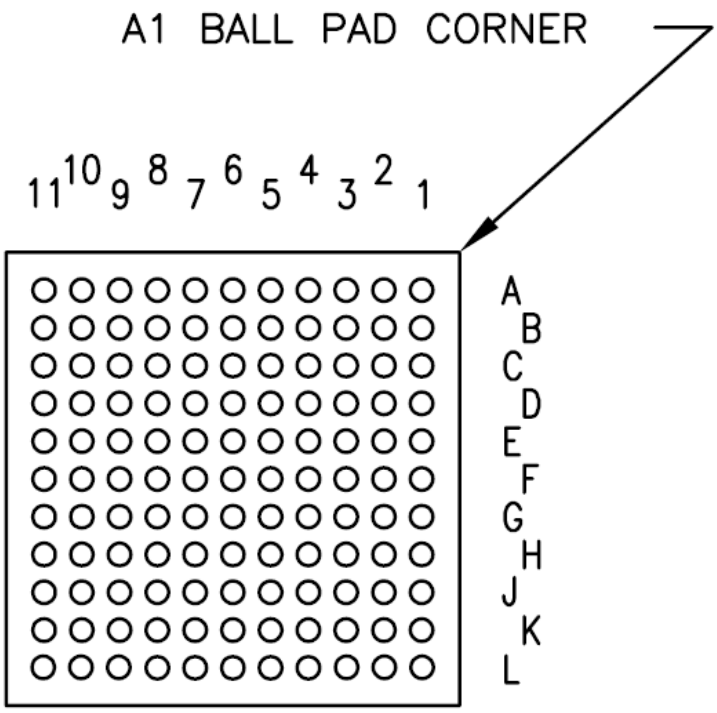
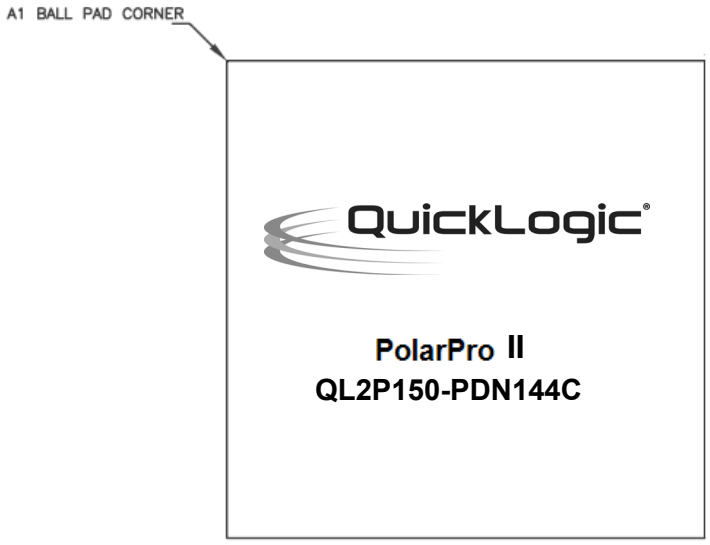


PolarPro II QL2P150 – 144-Ball (5 mm x 5 mm) VFBGA Pinout Diagram

Top



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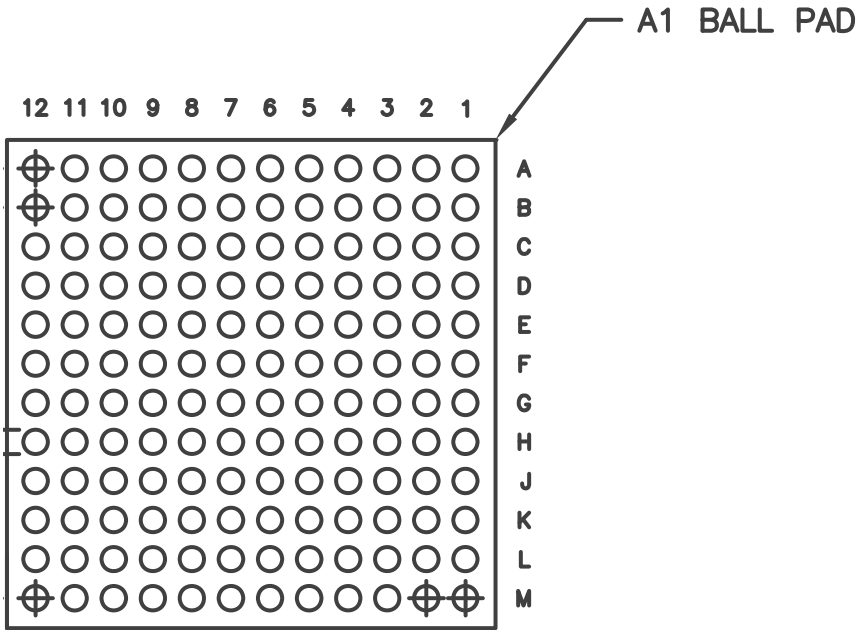
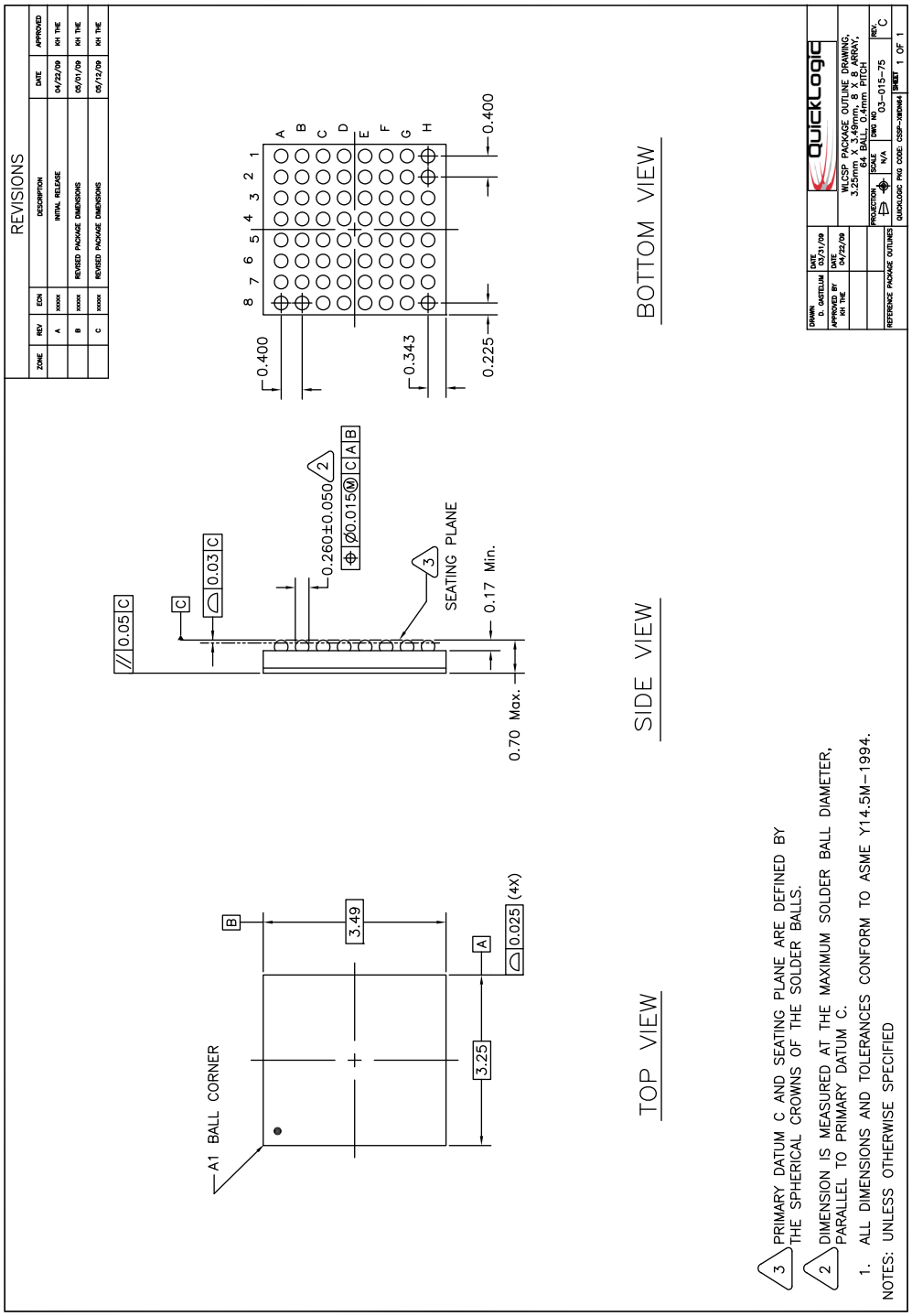
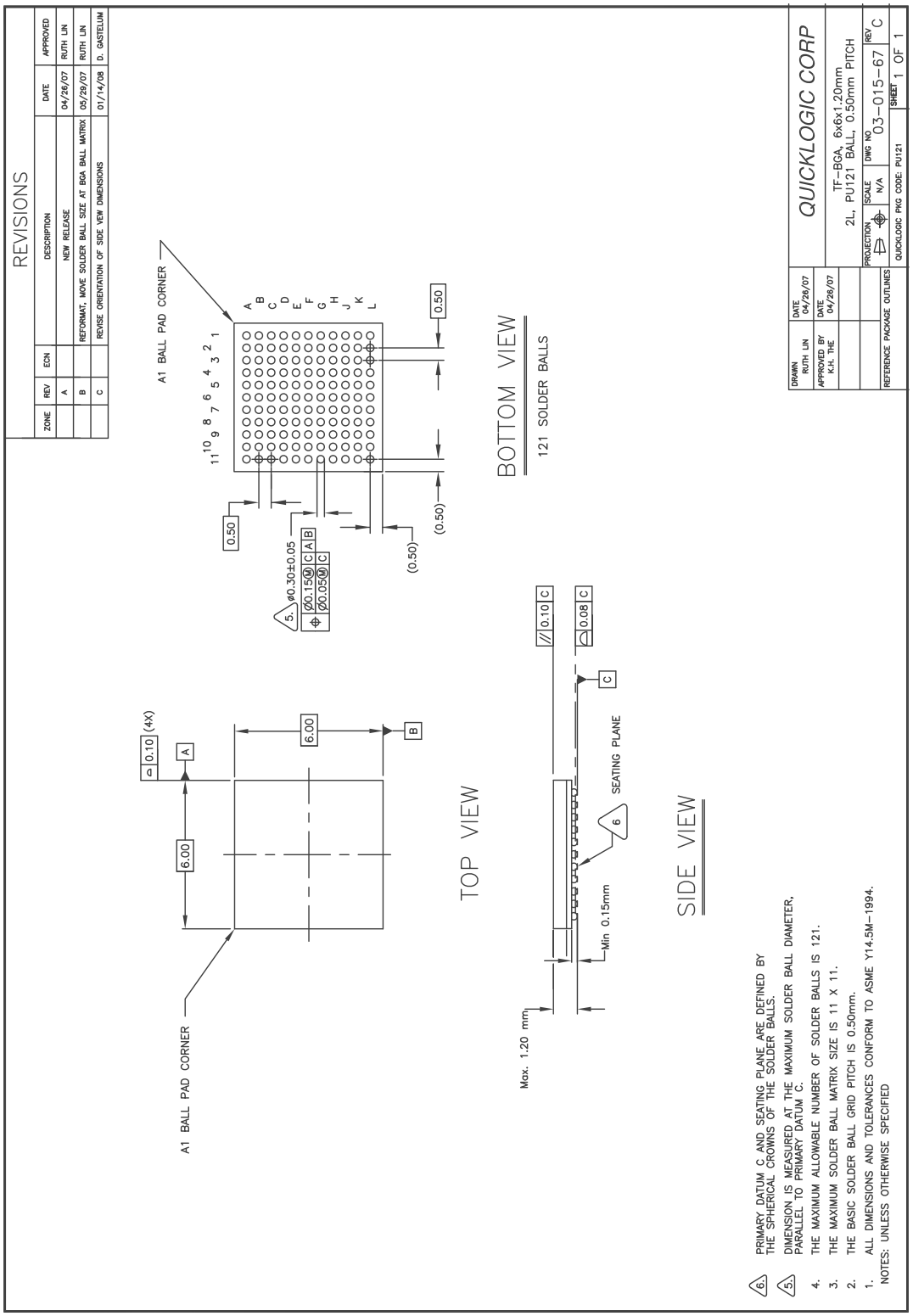


Package Mechanical Drawings

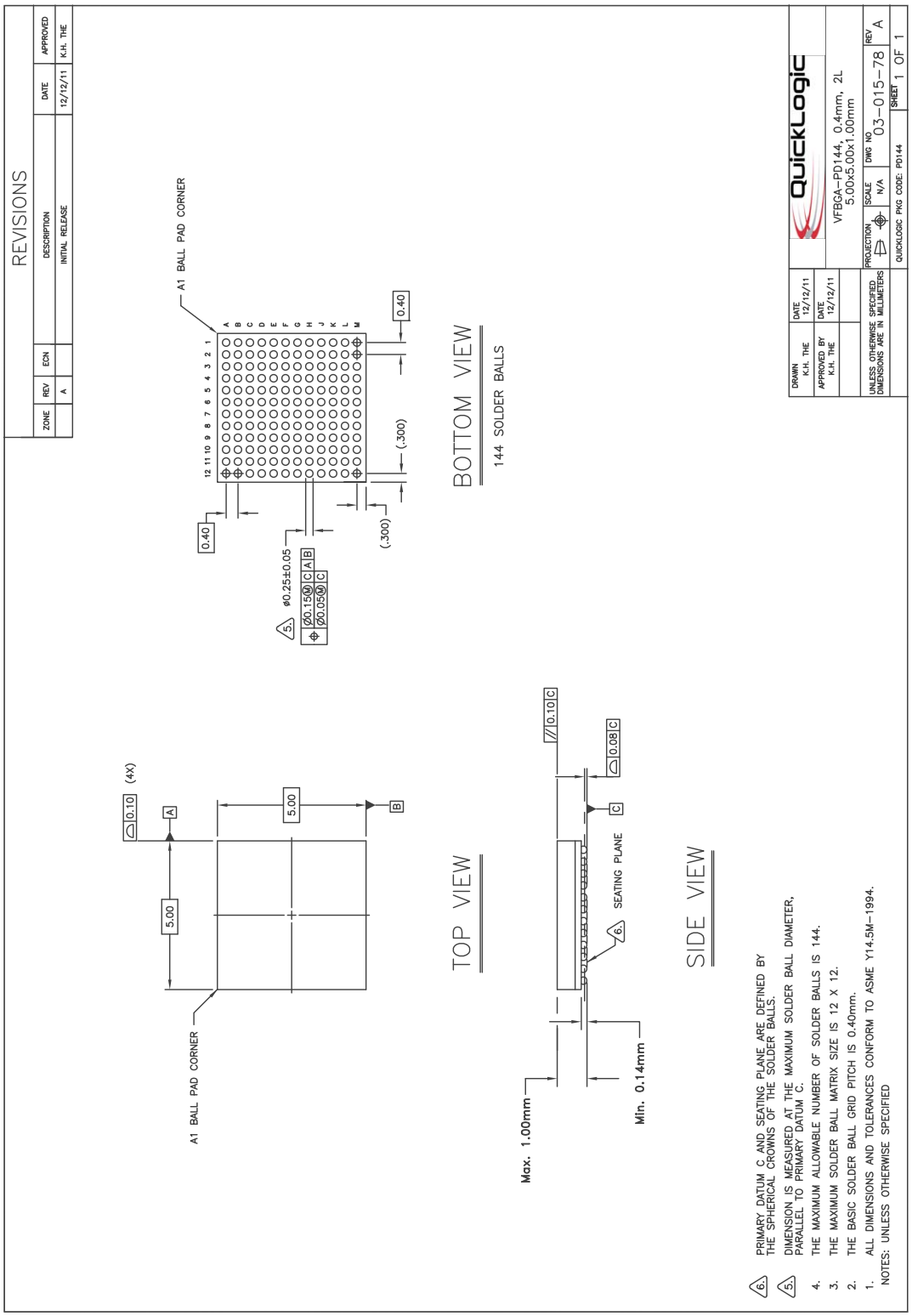
64-Ball (3.25 mm x 3.49 mm) WLCSP Package Drawing



121-Ball TFBGA (6 mm x 6 mm) Packaging Drawing



144-Ball VFBGA (5 mm x 5 mm) Packaging Drawing



Packaging Information

The PolarPro II QL2P150 device packaging information is presented in **Table 31**.

Table 31: QL2P150 Packaging Options

QL2P150		
Device Information	**Ball**	**Pb-Free**
Package Definitions[a]	64 WLCSP (3.25 mm x 3.49 mm) Pitch - 0.40 mm	X
	121 TFBGA (6 mm x 6 mm) Pitch - 0.50 mm	X
	144 VFBGA (5 mm x 5 mm) Pitch - 0.40 mm	X

a. TFBGA = Thin Profile Fine Pitch Ball Grid Array
VFBGA = Very Fine Pitch Ball Grid Array
WLCSP = Wafer Level Chip Scale Package

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Revision History

Revision	Date	Originator and Comments
1.0	July 2013	Initial release.

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