Eclipse II Devices Errata

Ultra-Low Power FPGA Combining Performance, Density, and Embedded RAM

This document identifies all known bugs for the Eclipse II family devices as of the date printed at the end of this document. Each issue is numbered, named and tracked individually. A severity level is also identified for each issue and is defined as:

- **Low**—A workaround exists and can be implemented in software
- **Medium**—A workaround exists and can be implemented in hardware
- **High**—No workaround exists at this time

For each issue, the affected device part numbers and silicon revision (if applicable) are identified. Also when applicable, workarounds for each issue are explained. Workarounds are fixes that can be implemented by the designer (designers can also contact QuickLogic for assistance). Resolutions for each issue are also identified, indicating when the issue will be fixed by QuickLogic (in a future revision of the device).

Issue #	Eclipse II.1
Title	Vded Pin Labeling
Severity	Medium
Affects	Eclipse II QL8325 and QL8250 device pinout tables in Rev A, B, D and E of the Eclipse II Family Datasheet. This document pertains only to Rev A, B, D, and E and previous versions of the datasheet; Rev C and F have the correct pin table information.
Problem Description	In Rev E and previous versions of the Eclipse II Family Datasheet, the pins shown in Table 1 were labeled Vcc. They are actually Vded pins. Vded pins specify the input tolerance of the dedicated JTAG, CLOCK and IOCTRL pins, and the output drive of the JTAG pins. Table 1. Updated Pin Tables Device / Package / Mislabeled Pins QL8250 / PQ208 / 79, 184 PT280 / H16, K1 PS484 / E11, V12 QL8325 / PQ208 / 79, 184 PT280 / H16, K1 PS484 / E11, V12
Resolution	The previously mentioned pins are the voltage supply pins for the JTAG I/O inside Eclipse II devices. If Rev A, B, D or E of the datasheet was used for board layout, these pins may have been connected to Vcc (1.8 V). If JTAG and/or the PROM Loading feature are not used, it is acceptable to continue to connect these pins to Vcc (1.8 V). If JTAG and /or the PROM Loading feature are used and the JTAG pins are driven to 3.3 V, current will flow through the JTAG pin circuitry; the device will still be functional, but the overall lifetime of the device will be shortened.

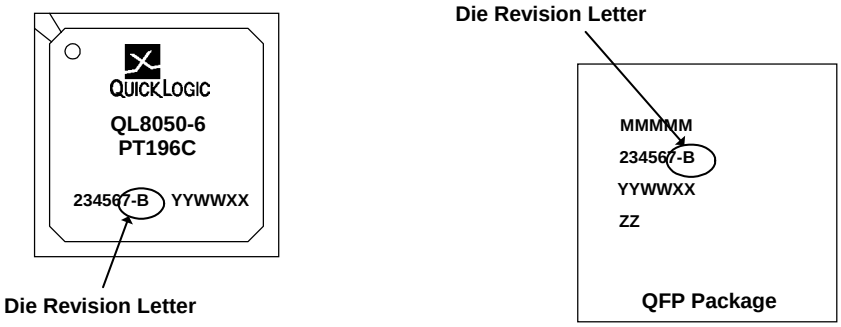
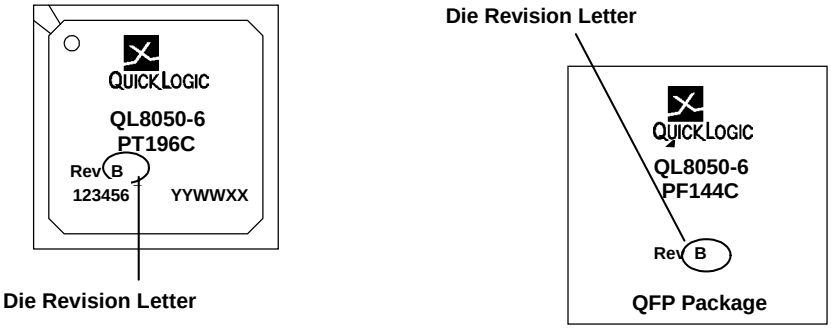
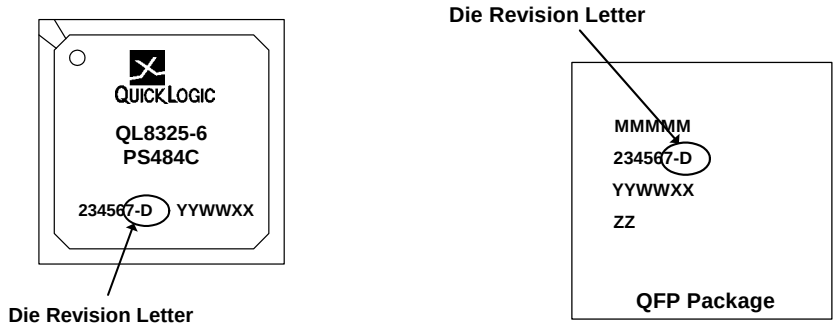
<table>
<tr><th>Issue #</th><th>Eclipse II.2</th></tr>
<tr><td>Title</td><td>ESD Pad Protection Specification</td></tr>
<tr><td>Severity</td><td>N/A</td></tr>
<tr><td>Affects</td><td>Eclipse II devices with die revisions equal to or prior to the ones shown in Table 2.
Table 2. Die Revision
<table><tr><th>Device</th><th>Die Revision with Condition</th></tr><tr><td>QL8150</td><td>B</td></tr><tr><td>QL8050</td><td>B</td></tr><tr><td>QL8025</td><td>B</td></tr></table>The die revision code locations are shown in Figures 1 and 2. QFP packages are marked on the top or bottom and BGA packages are marked on the top.
Figure 1. Location on Package Marking for Die Revision
 

Figure 2. Alternative Location on Package Marking for Die Revision
 
</td></tr>
<tr><td>Problem Description</td><td>The ESD sensitivity level for all devices with the die revisions shown in Table 2 is JEDEC Class IC.
The ESD sensitivity level for all devices with die revision shown in Table 3 is 750 V JEDEC.
Table 3. Die Revision
<table><tr><th>Device</th><th>Die Revision with Condition</th></tr><tr><td>QL8325</td><td>G</td></tr><tr><td>QL8250</td><td>G</td></tr></table></td></tr>
<tr><td>Resolution</td><td>N/A</td></tr>
</table>

Issue #	Eclipse II.3
Title	SYNCRAM
Severity	**Medium**
Affects	Eclipse II devices with die revisions equal to or prior to the ones shown in Table 4. Table 4. Die Revision Device — Die Revision with Condition QL8150 — B QL8050 — B QL8025 — B The die revision code locations are shown in Figure 3. QFP packages are marked on the underside and BGA packages are marked on the bottom. Figure 3. Location on Package Marking for Die Revision 
Problem Description	The Embedded SRAM blocks in all Eclipse II devices with die revisions less than or equal to the ones listed in Table 4 have the following issues: • The WCLK and RCLK inputs to the RAM must be clocked with the same clock signal, OR, • If the WCLK and RCLK inputs to the RAM are clocked with separate clock signals, the design must not have the RE and WE signals active at the same time (i.e., reading and writing the RAM at the same time), OR, • If the ASYNC Read mode is selected for the RAM, the Read Address cannot toggle within 1 ns of the rising edge of the WCLK input and the WE signal being active.
Resolution	Fixed in Die Revision F (and later).

Please contact our support team at www.quicklogic.com/support if you have further questions.

Revision History

Revision	Date	Originator and Comments
Rev. A	January 2005	Brian Faith, Mehul Kochar, and Kathleen Murchek Combined all existing Eclipse II errata into one document. Includes conversion from MS Word to FrameMaker format.
Rev. B	October 2008	Kathleen Murchek Updated Contact and Copyright info. Added Disclaimer.

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